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FIG.1

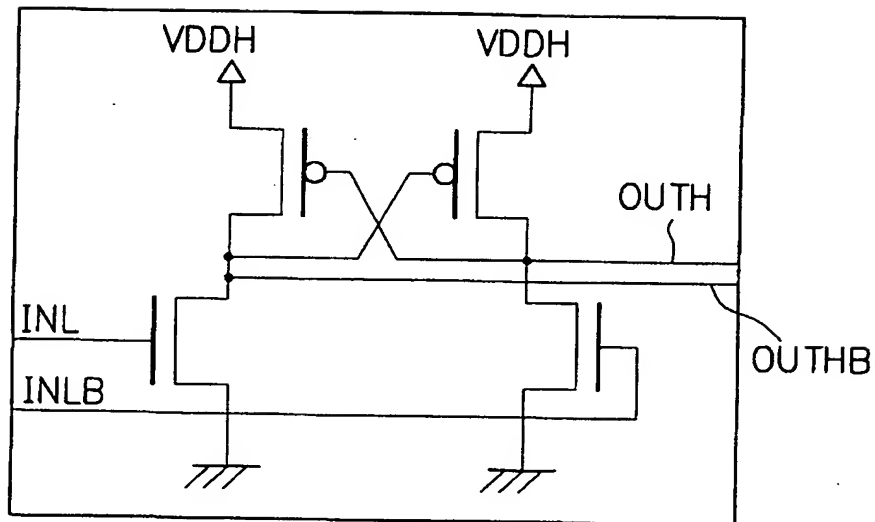
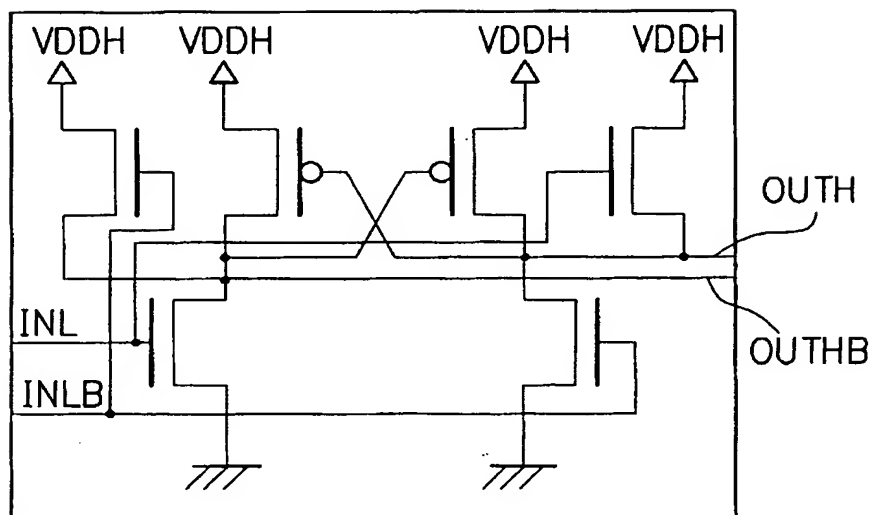


FIG.2



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FIG.3

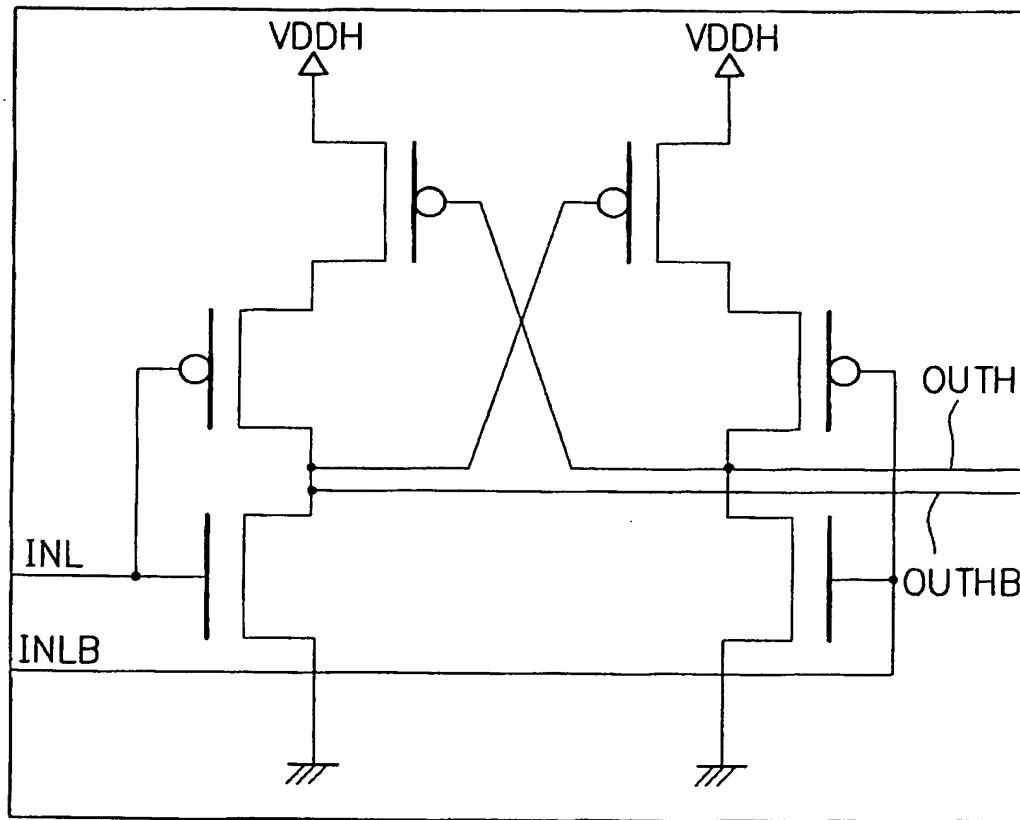


FIG.4

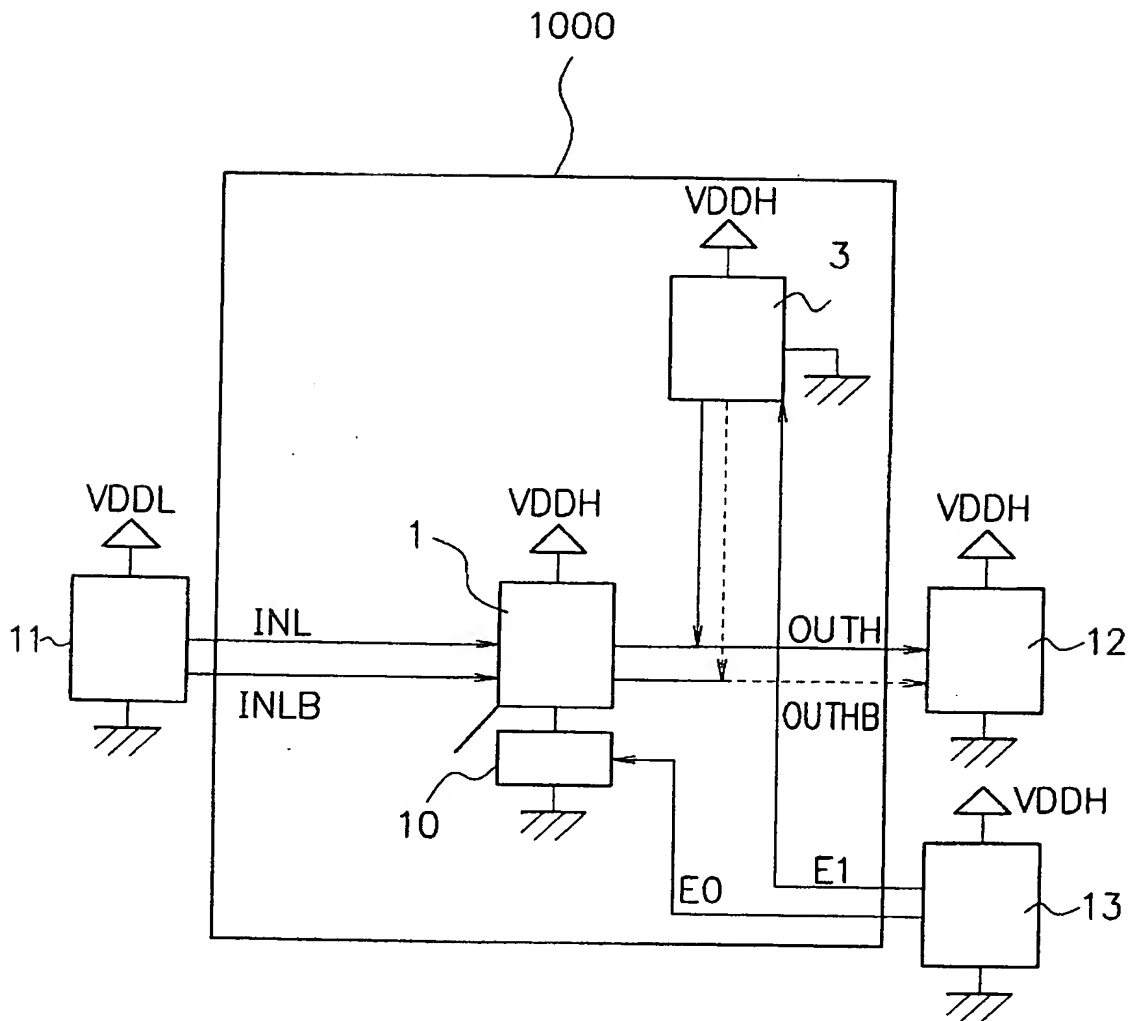
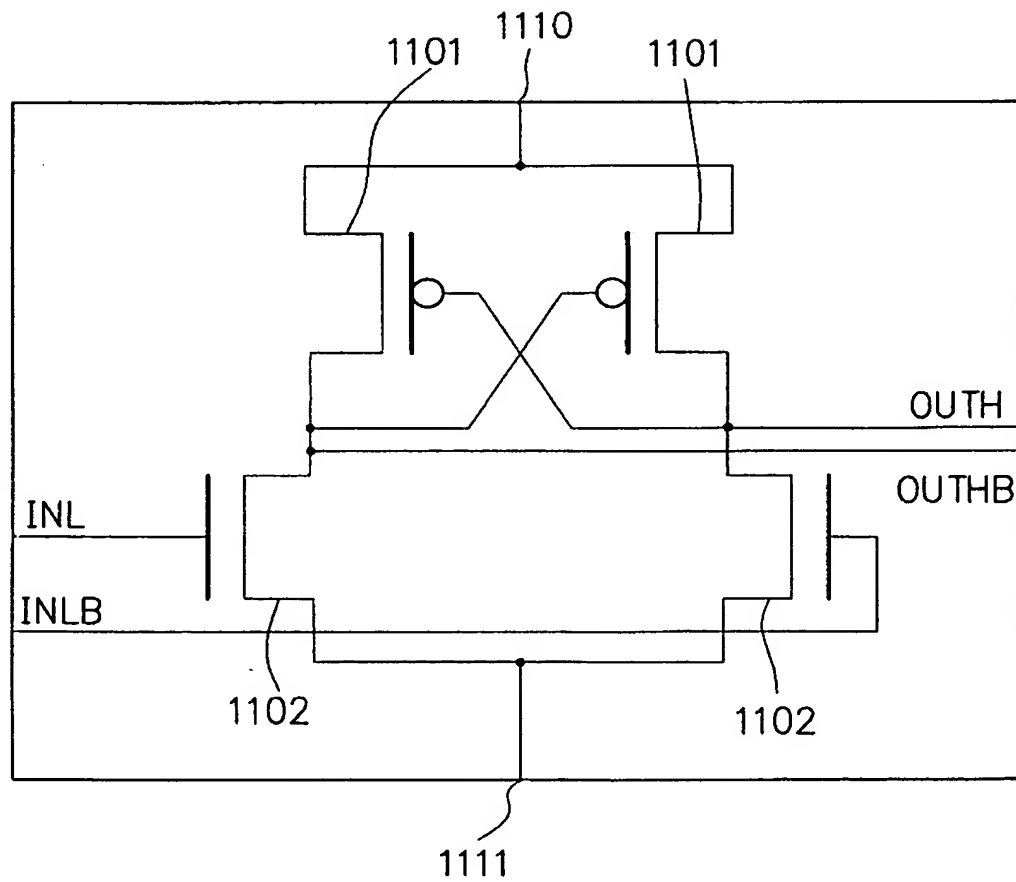


FIG.5



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FIG.6

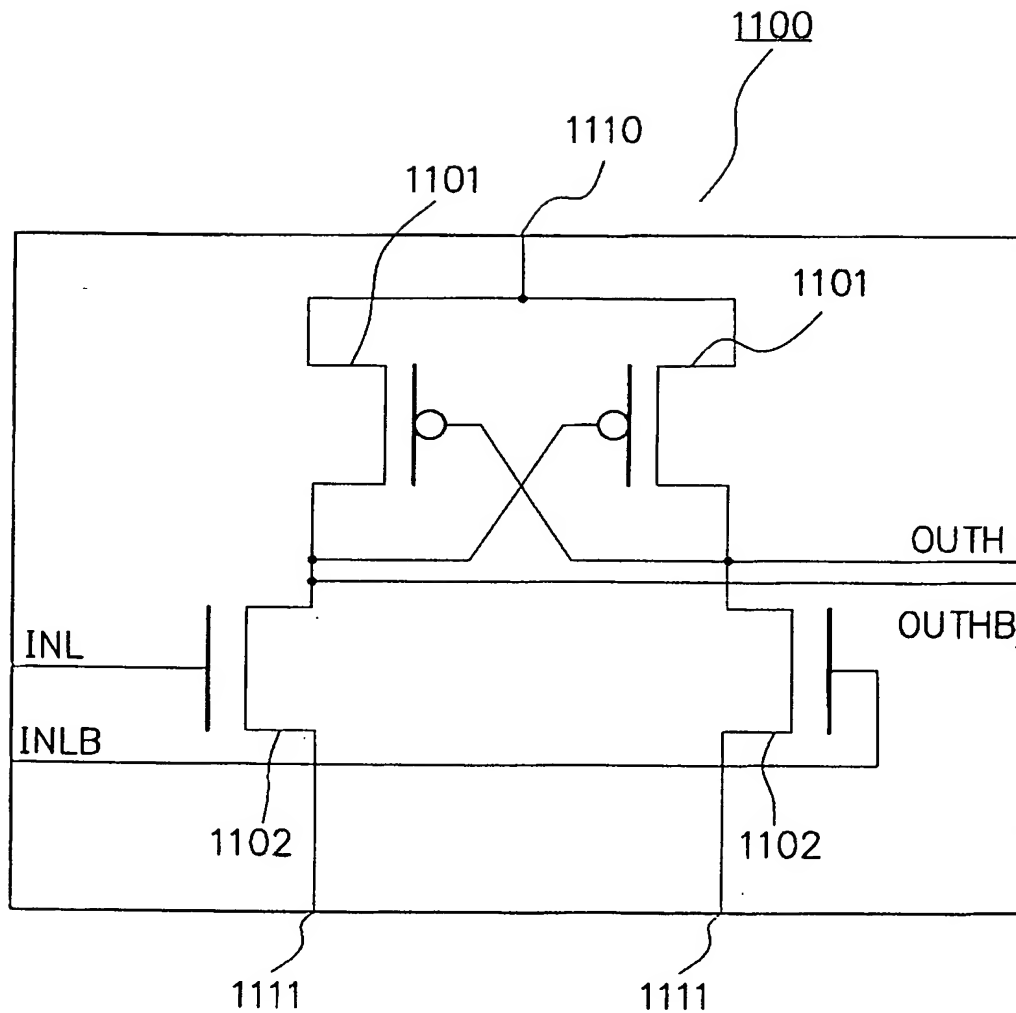


FIG. 7

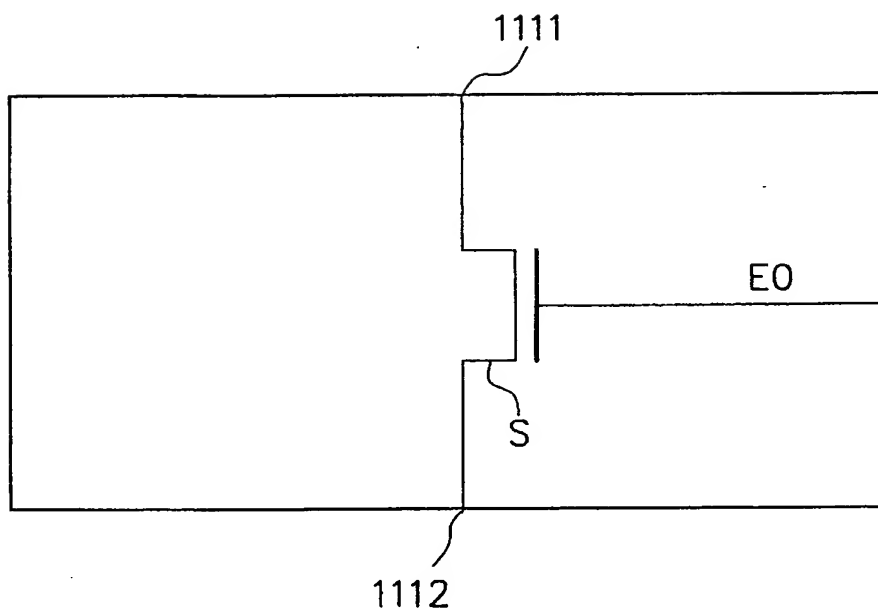
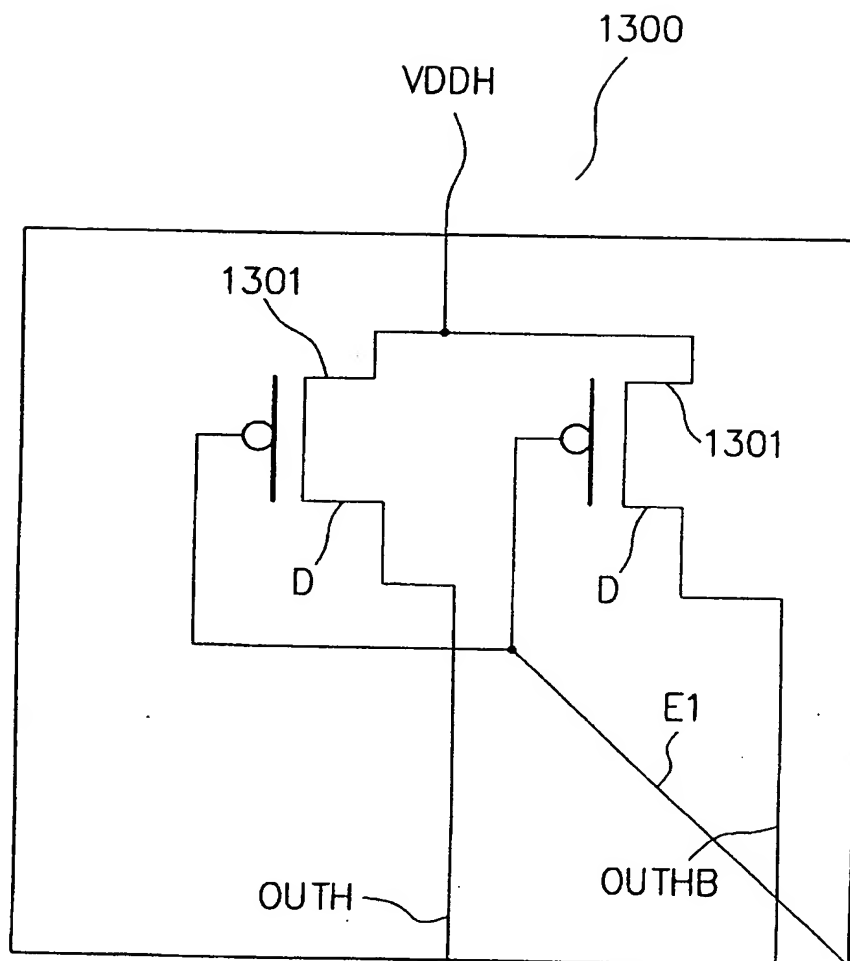


FIG.8

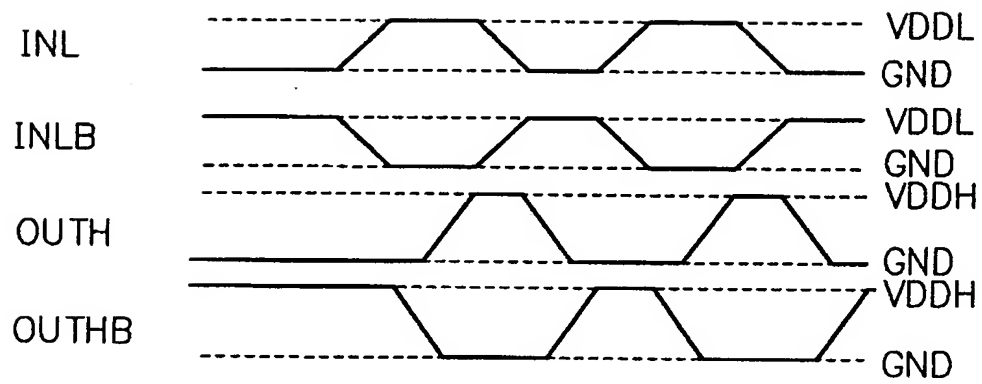




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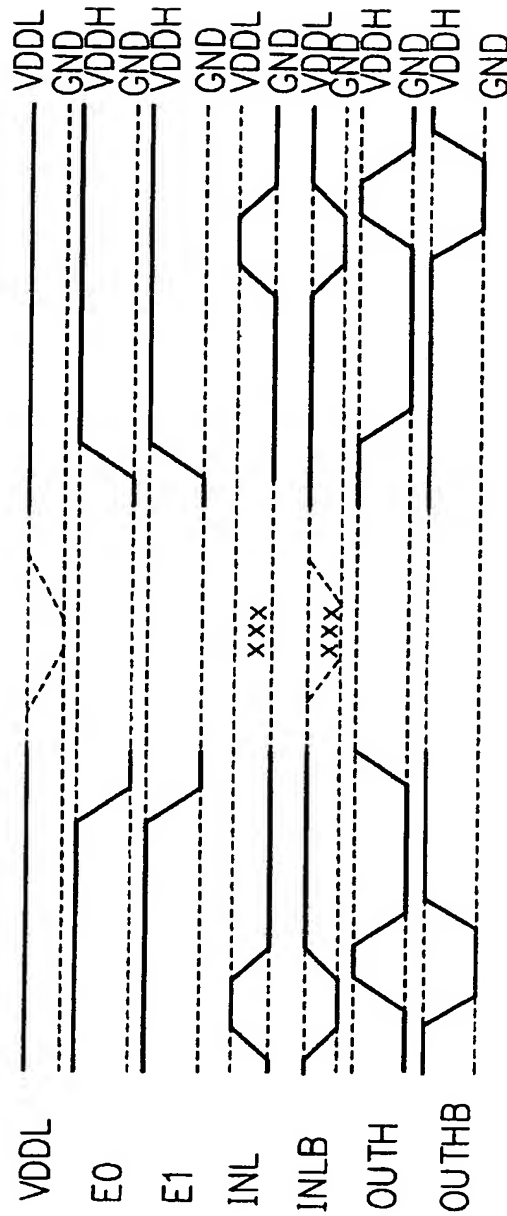
FIG.9



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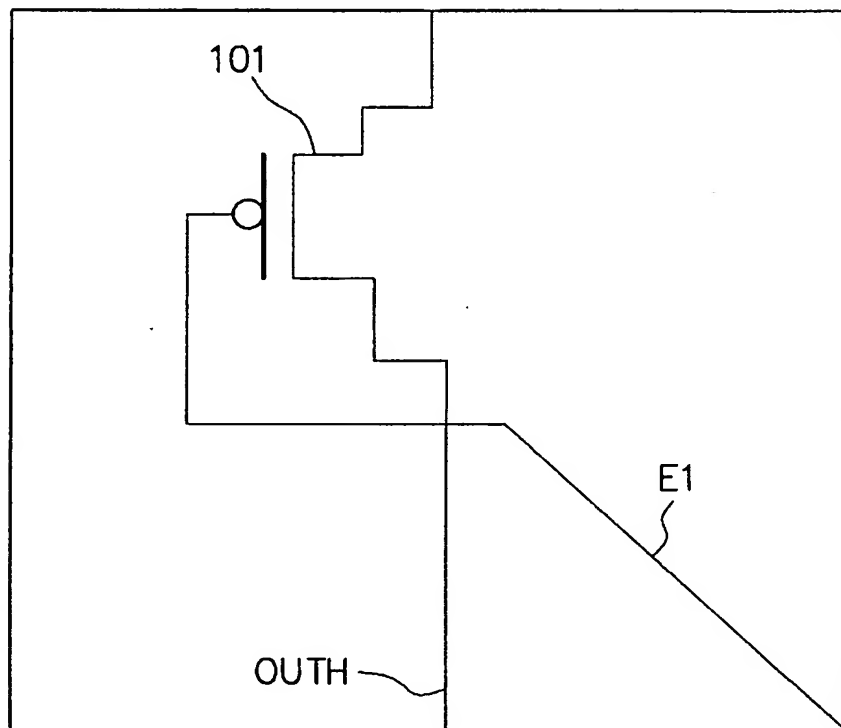
FIG.10



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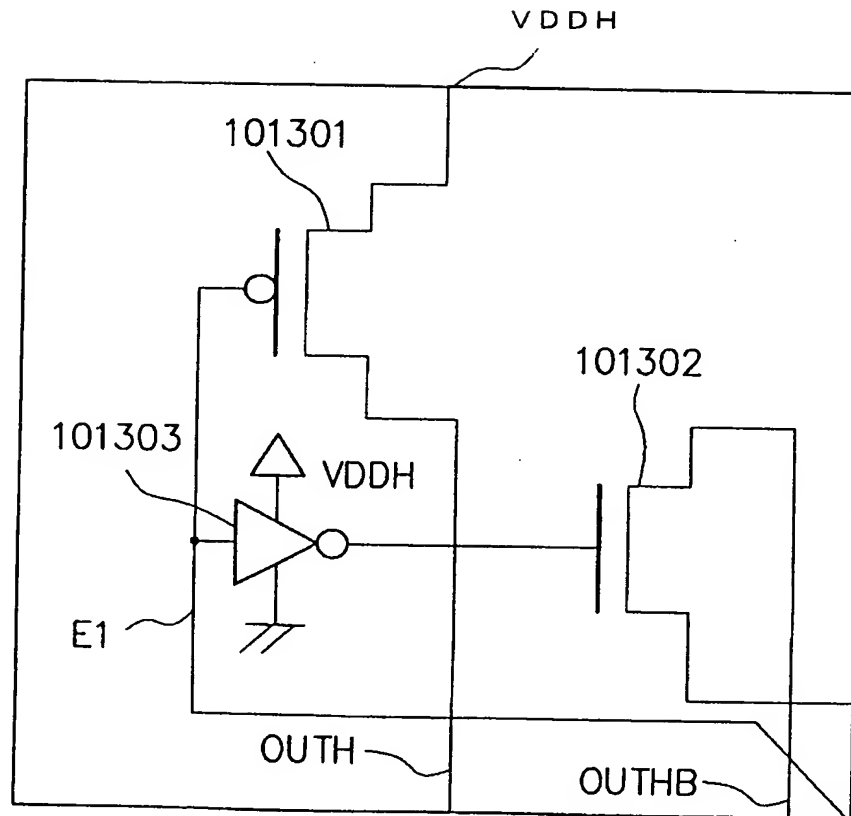
FIG.11



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FIG.12

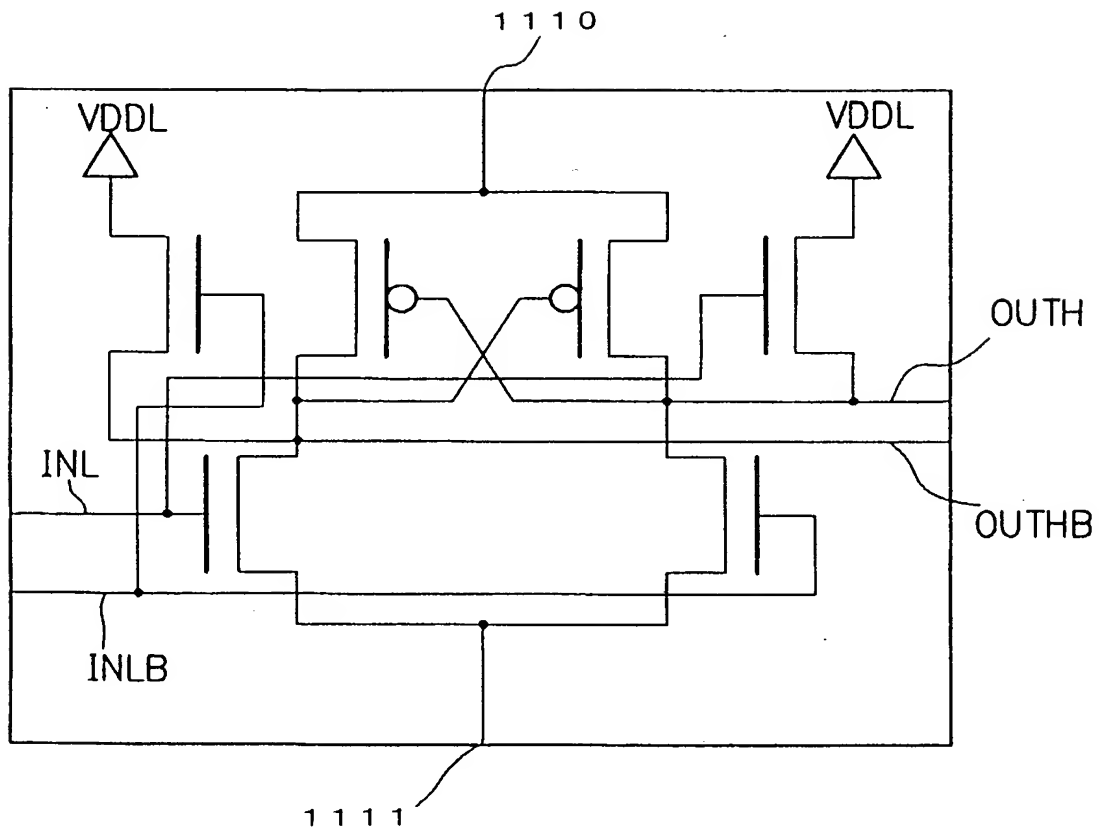


The diagram shows a CMOS inverter circuit. The input signal **E1** is connected to the input of an inverter. The inverter's output is connected to the gate of a PMOS transistor. The PMOS transistor's source is connected to **VDDH** and its drain is connected to the output node **OUTHB**. The output node **OUTHB** is also connected to the input of a buffer, which is represented by a square symbol with a diagonal line. The buffer's output is connected back to the input of the inverter, forming a feedback loop.

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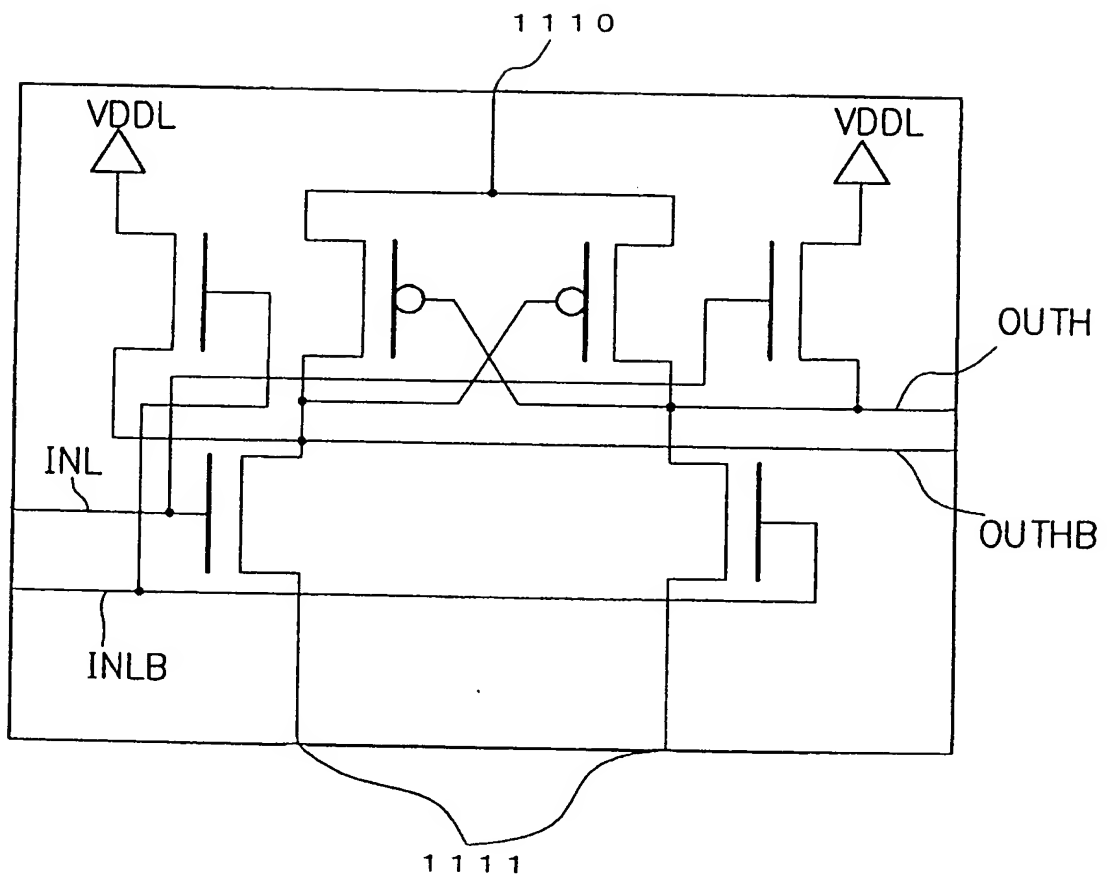
FIG.14



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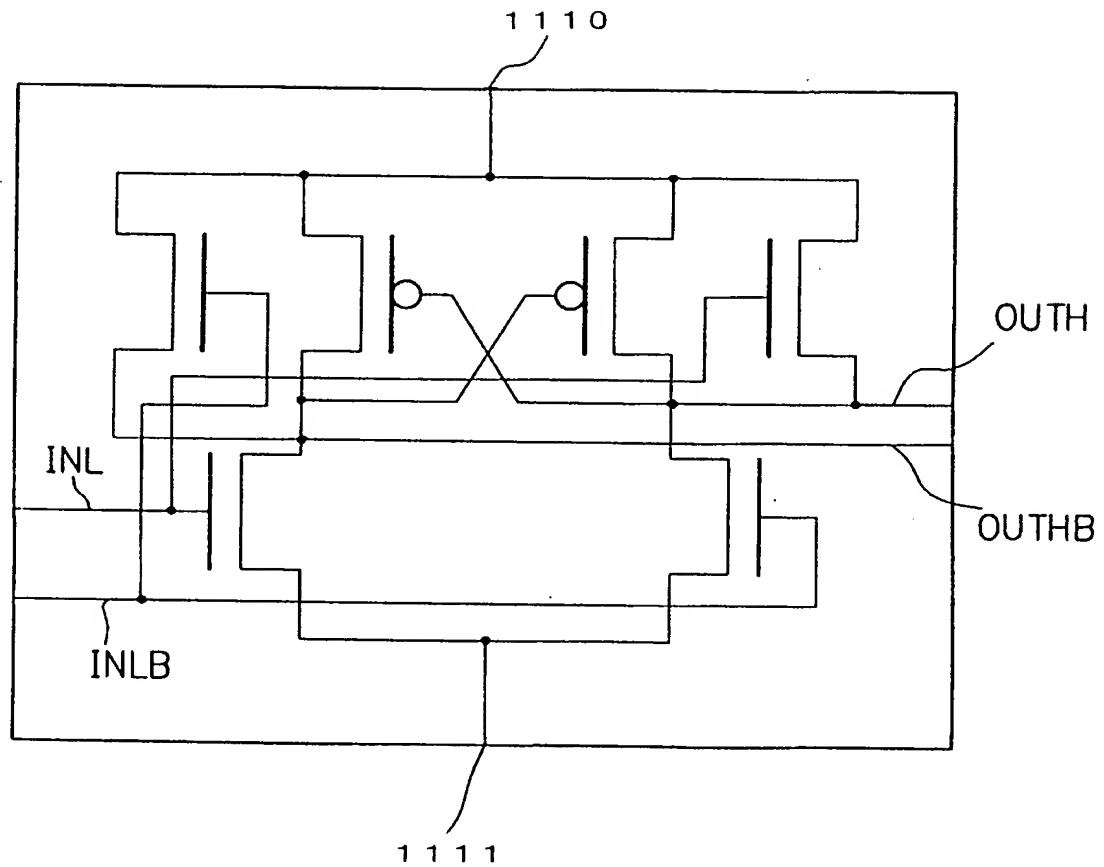
FIG.15



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FIG.16

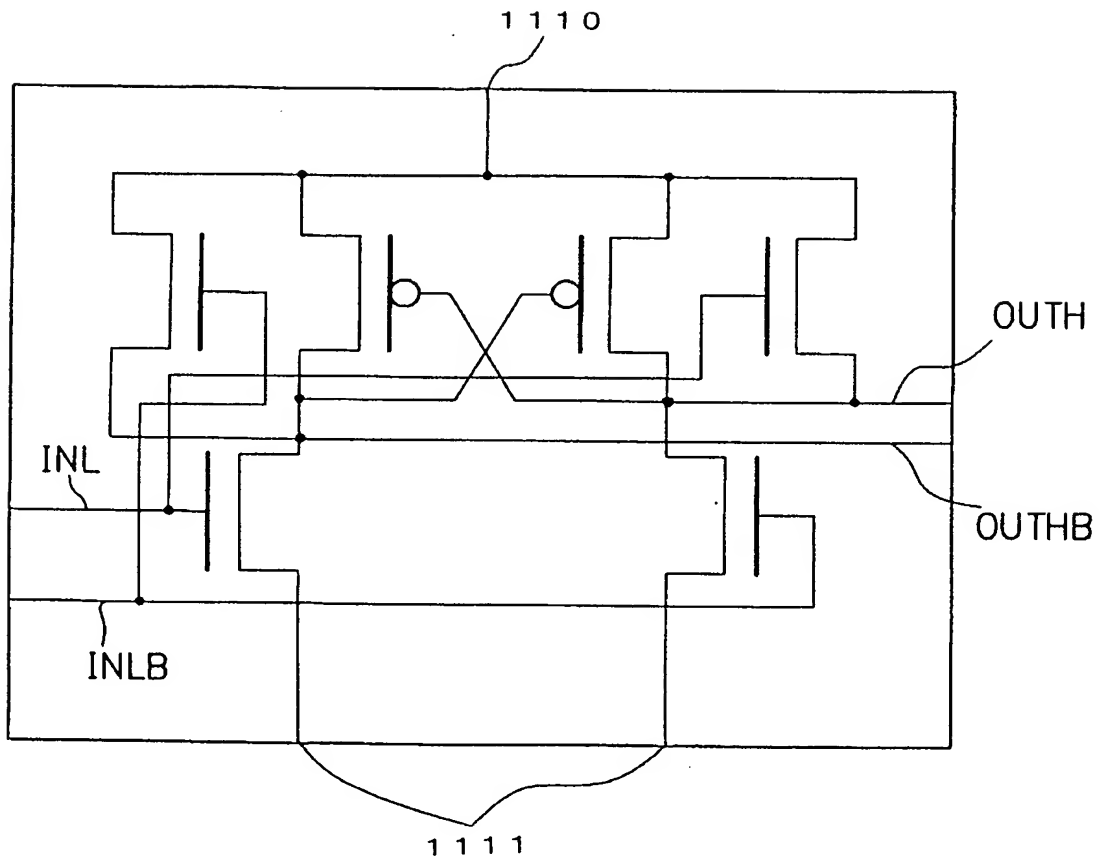




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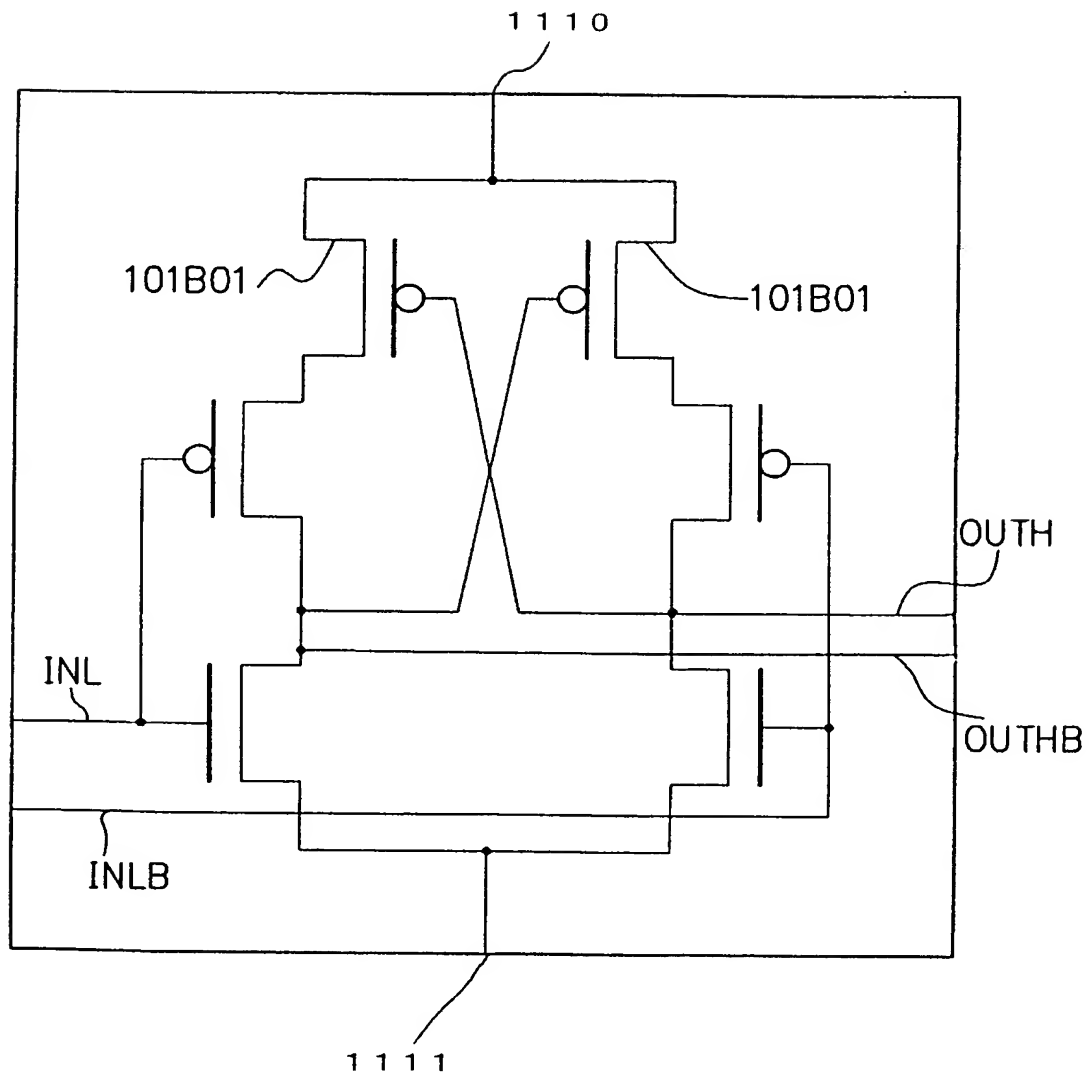
FIG.17



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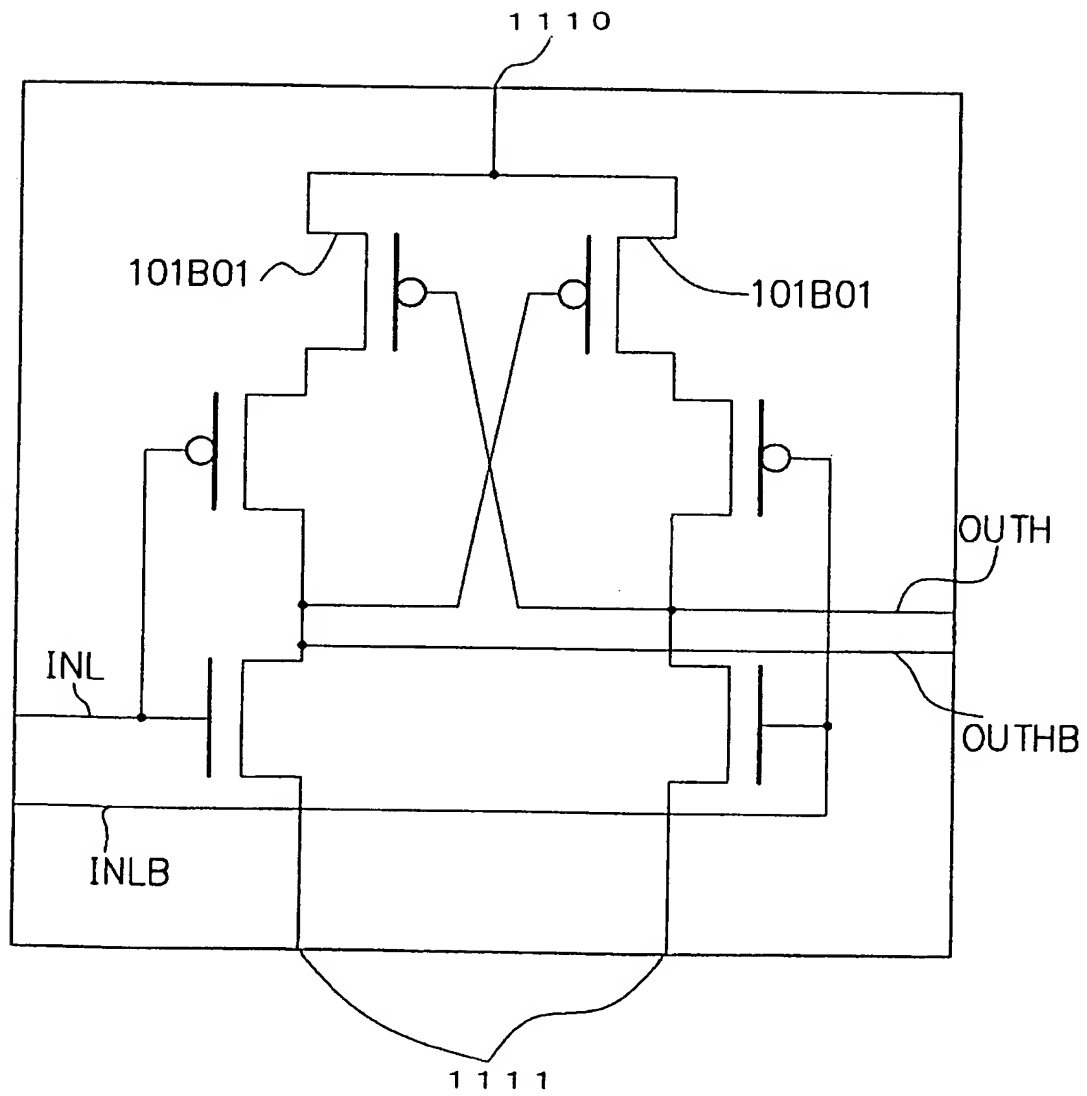
FIG. 18



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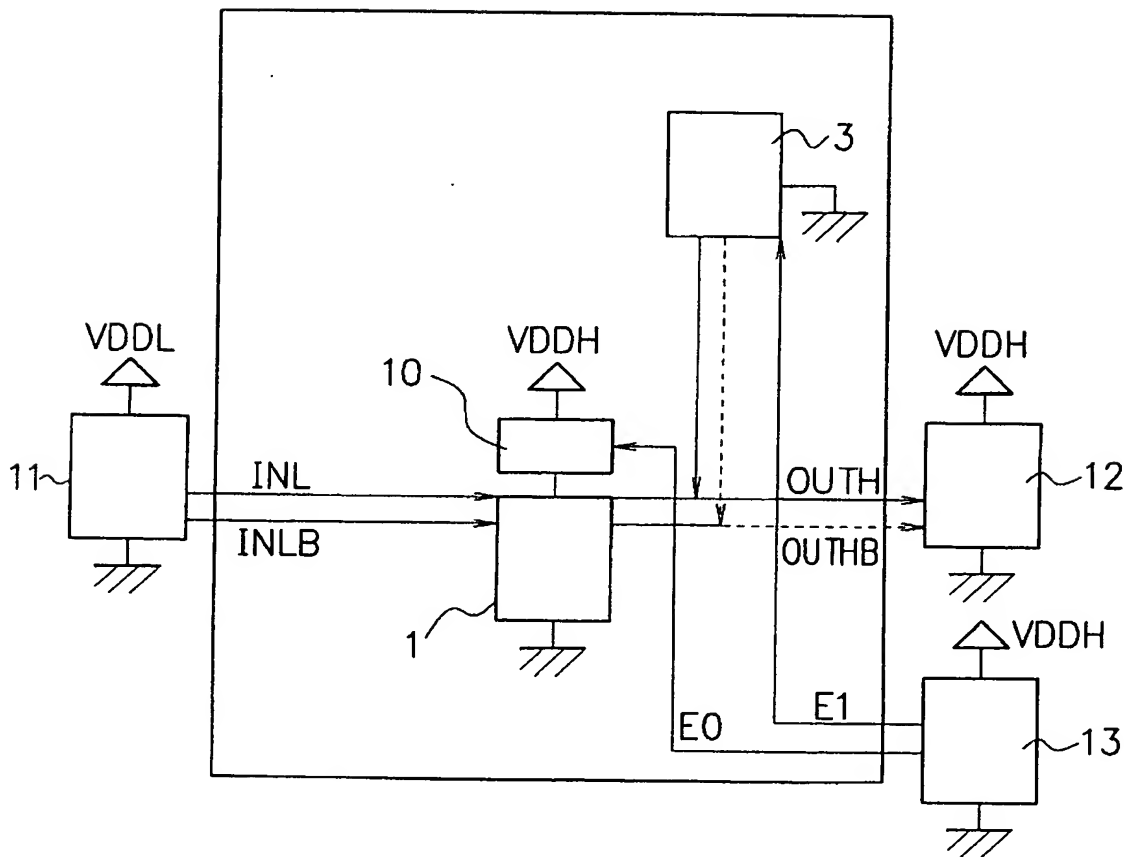
FIG.19



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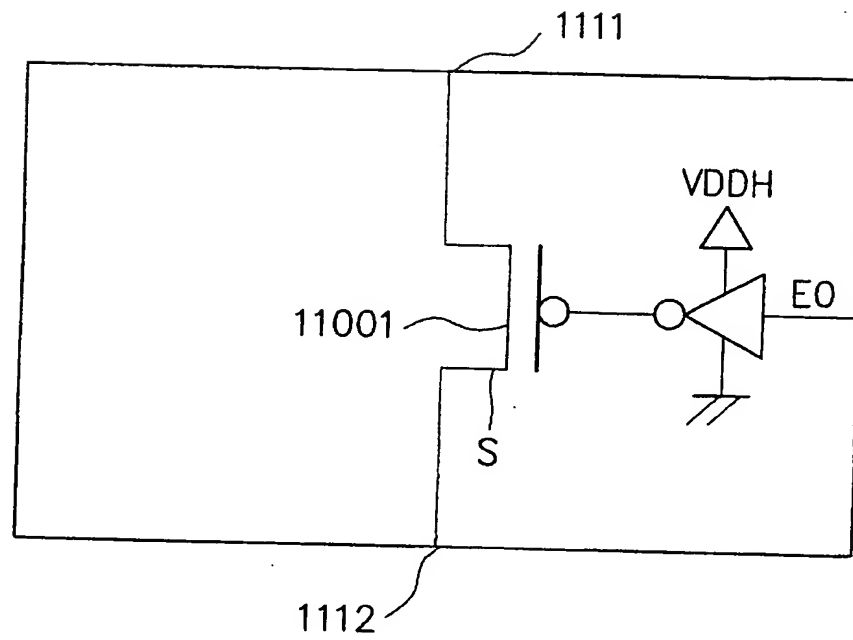
FIG.20



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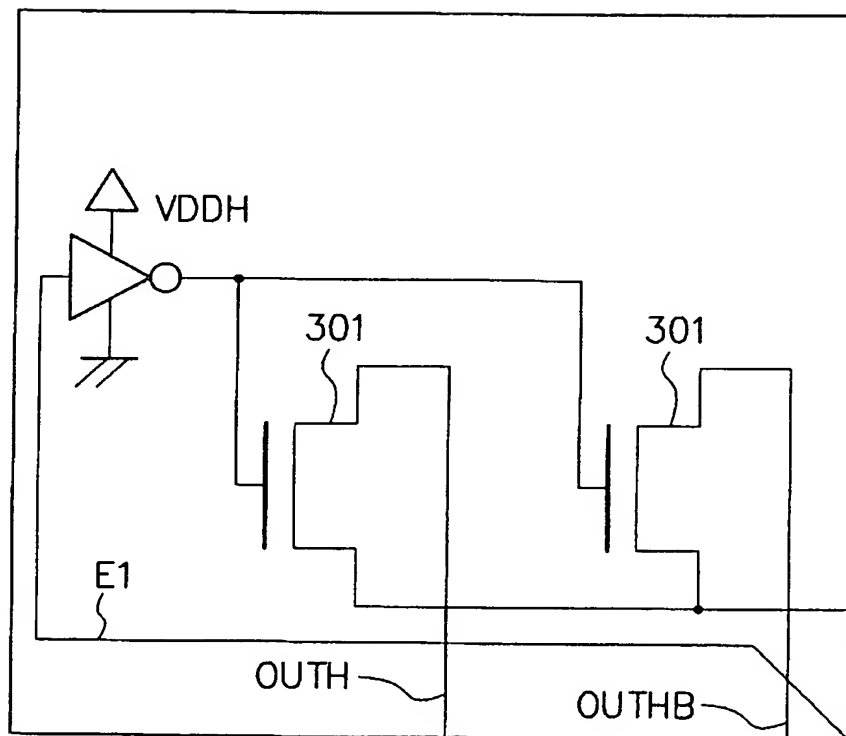
FIG.21



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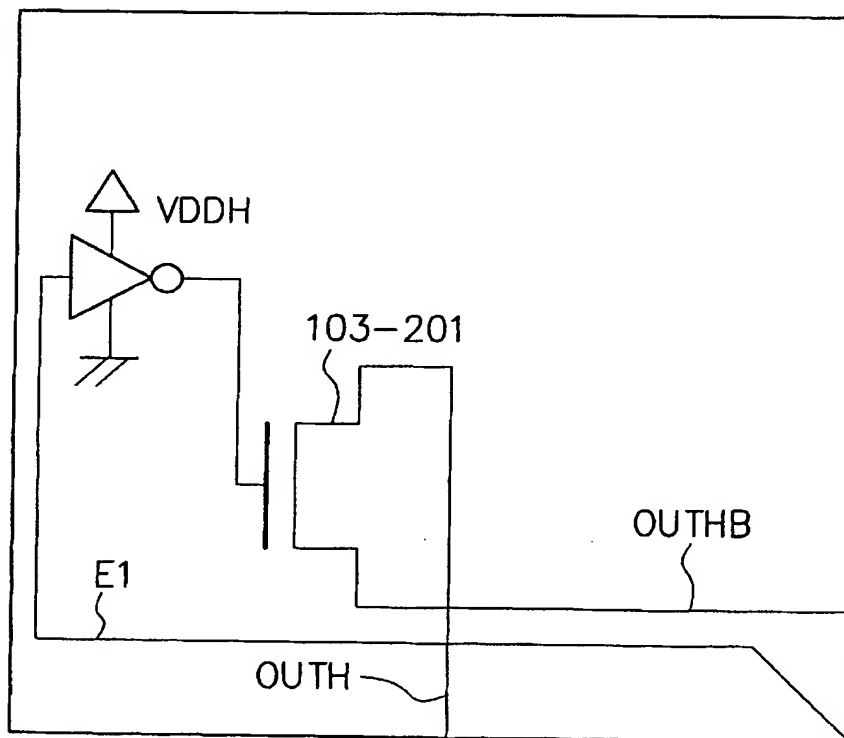
FIG.22



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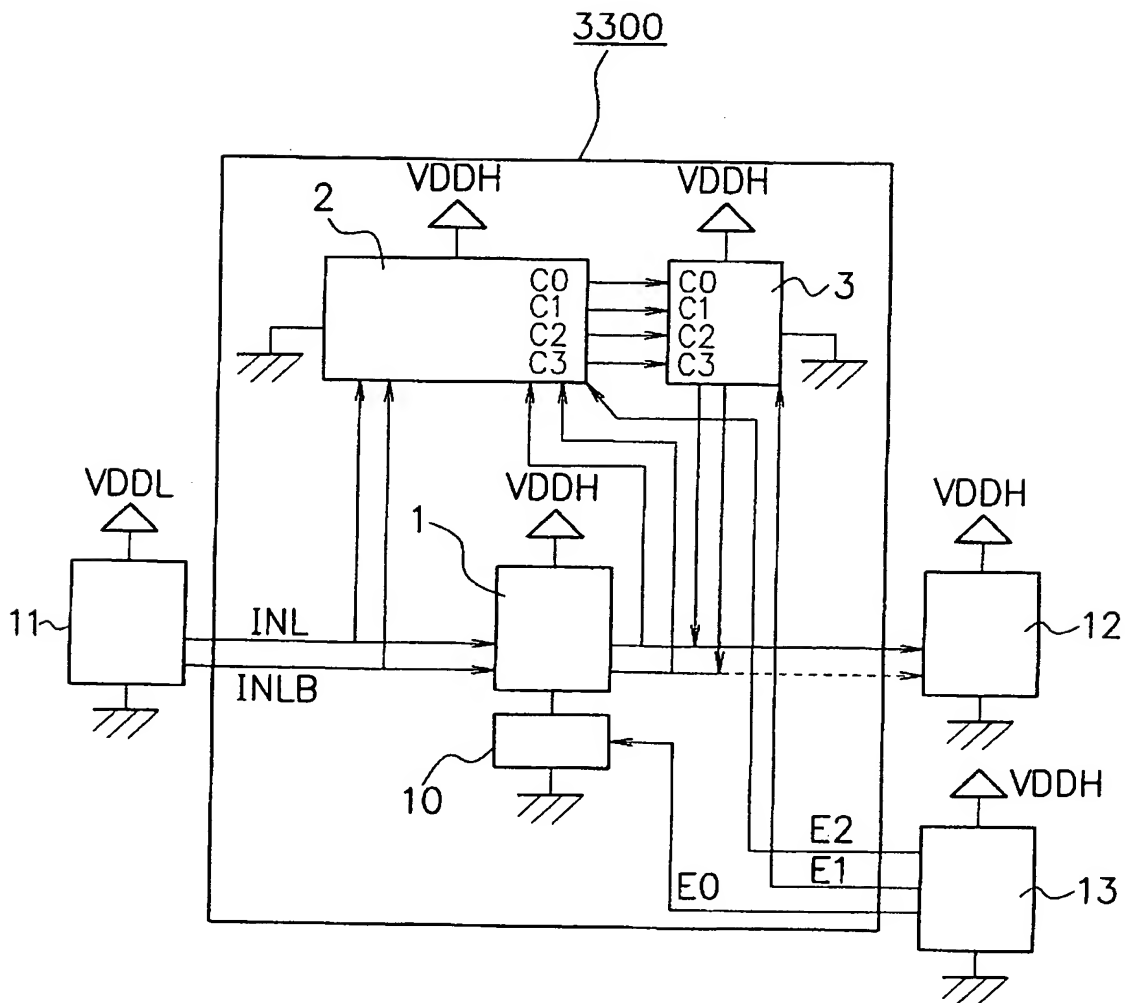
FIG.23



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FIG.24

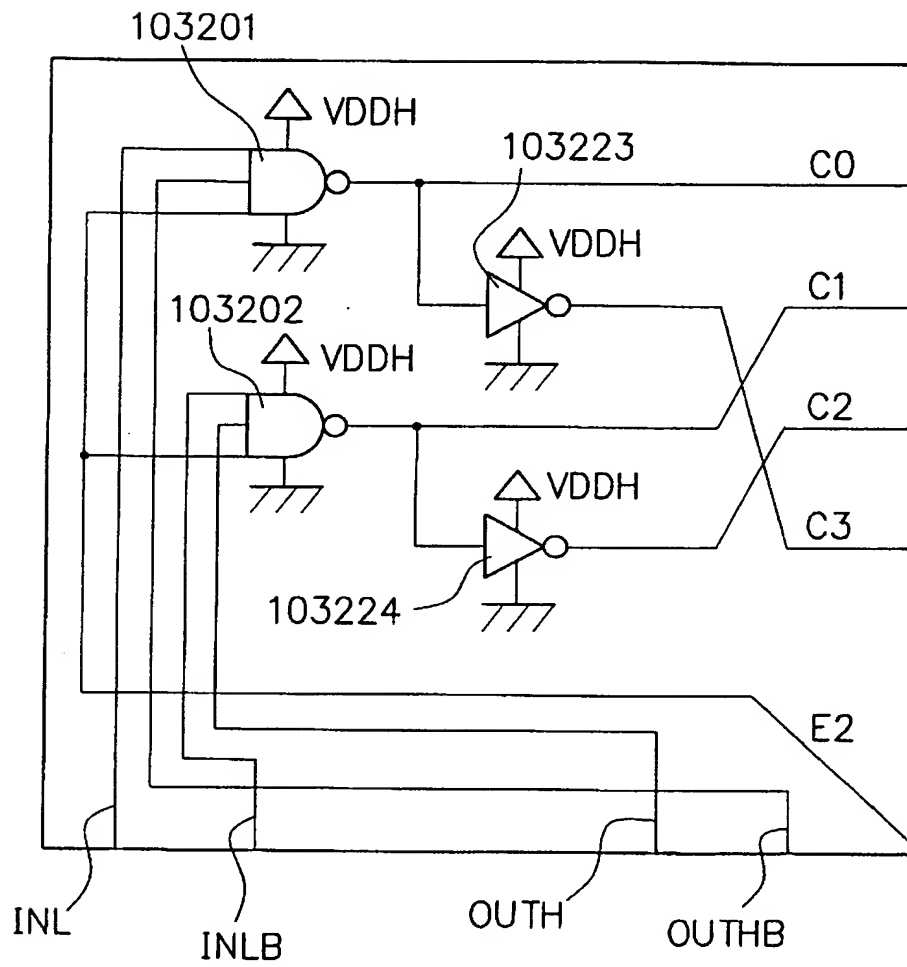




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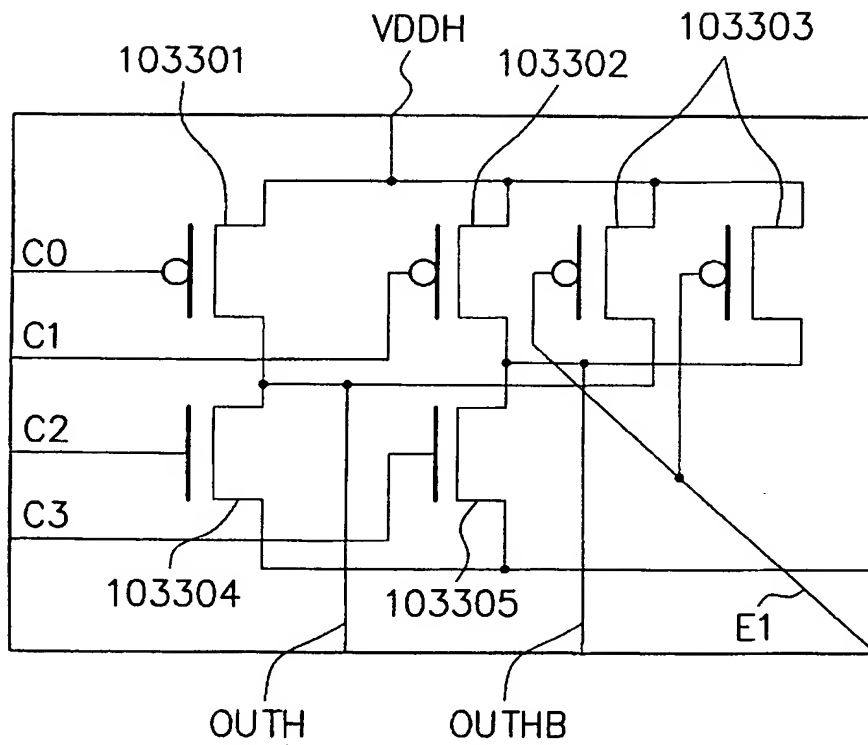
FIG.25



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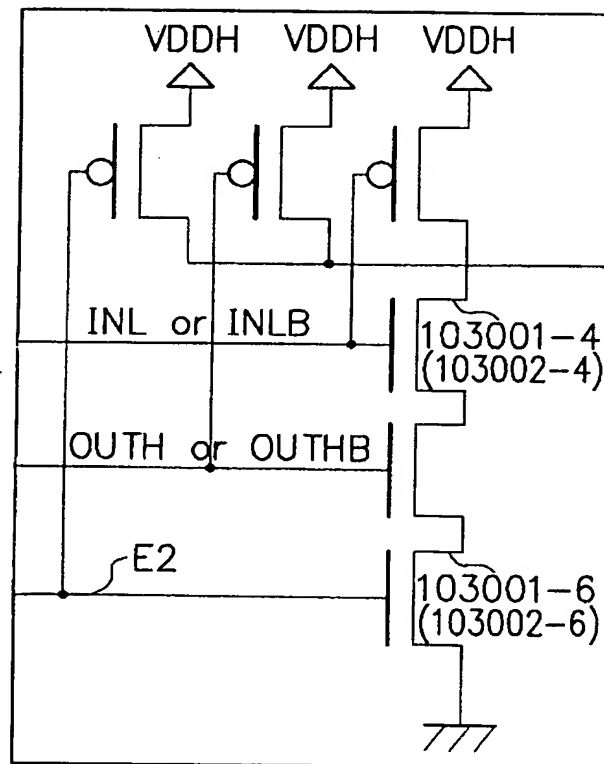
FIG.26



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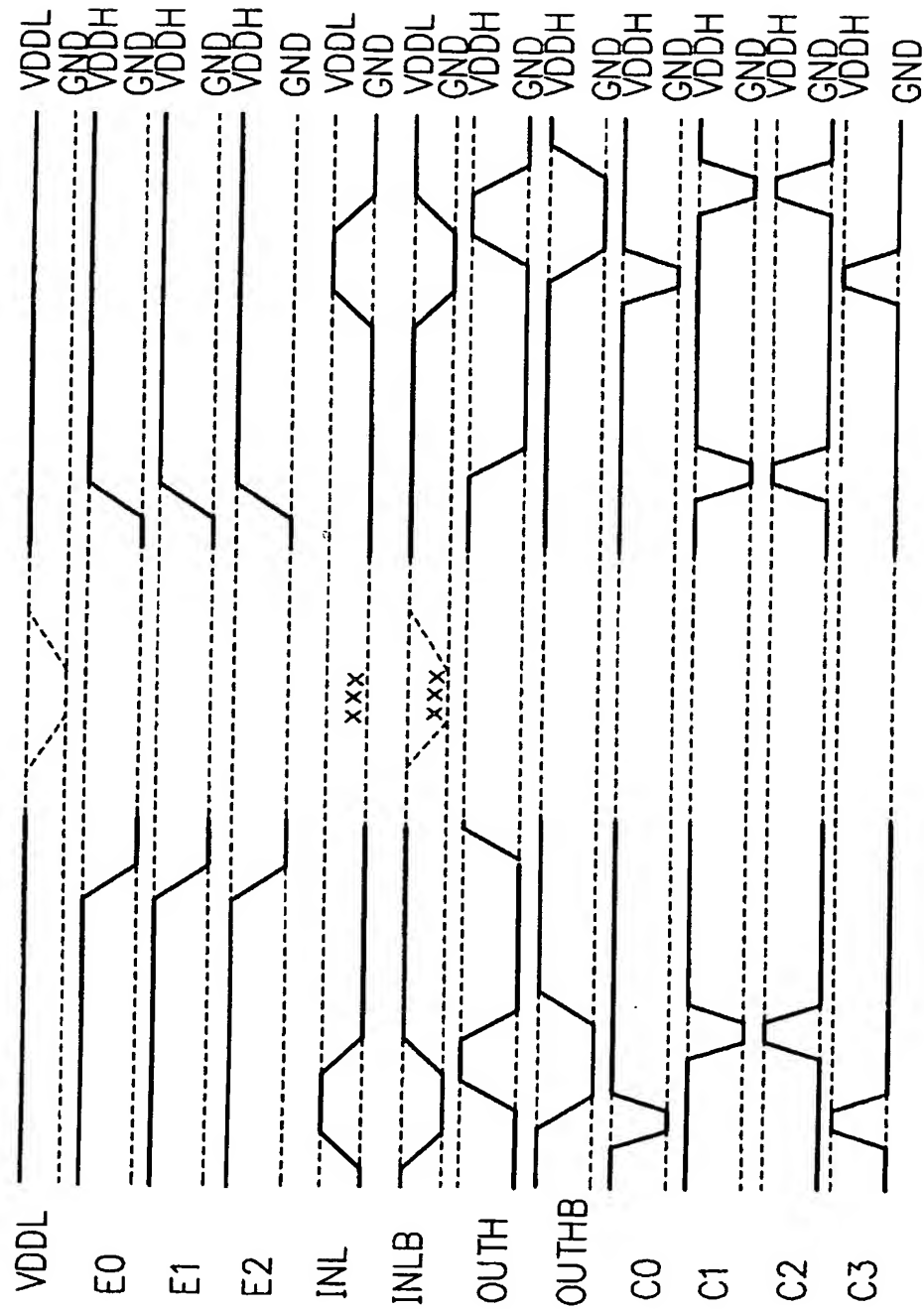
FIG.27



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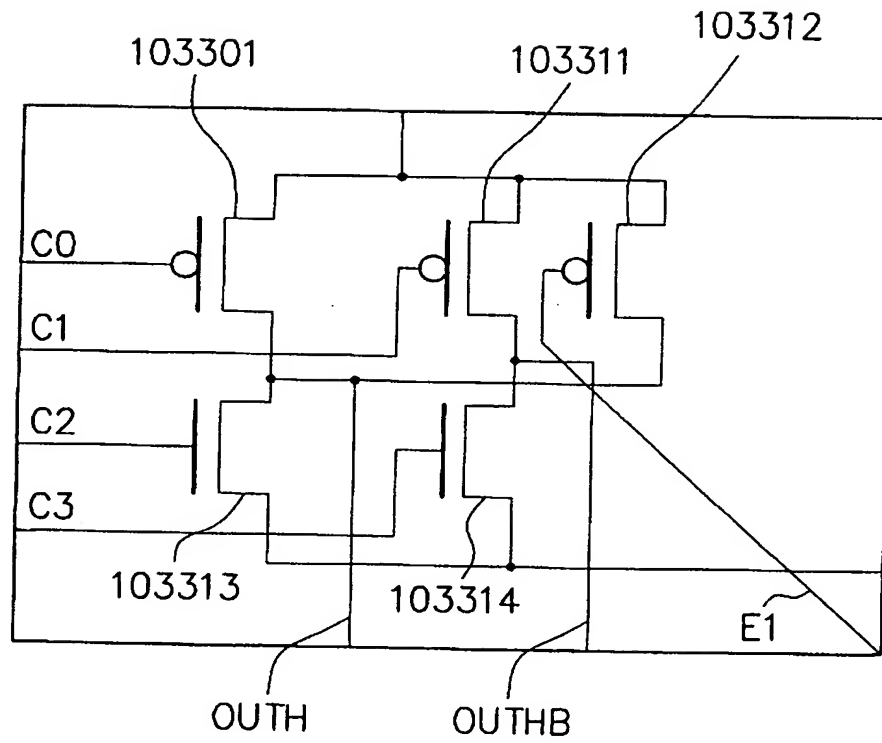
FIG.28



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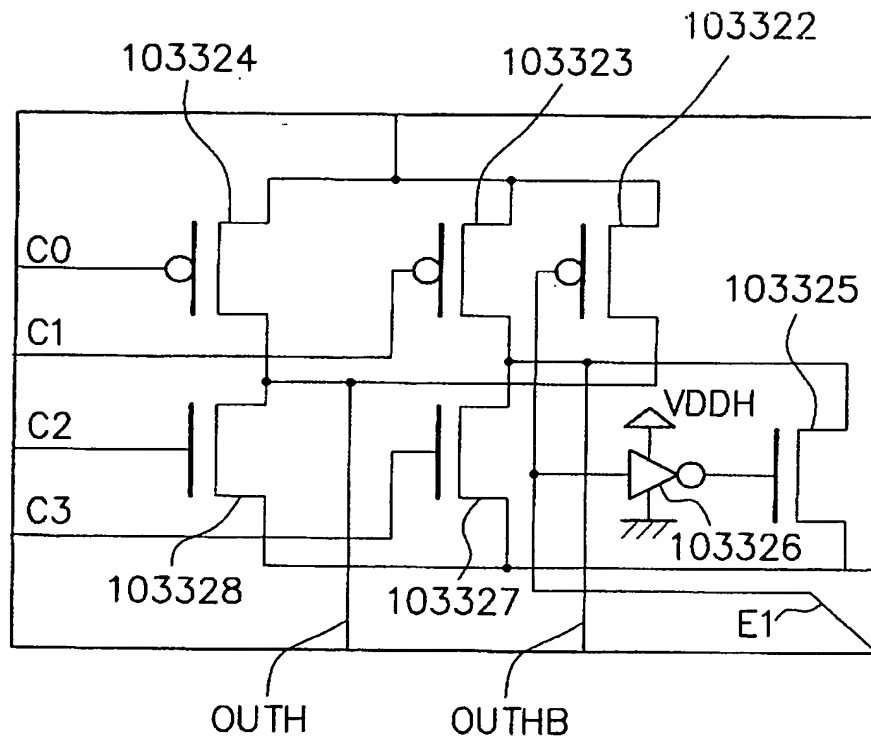
FIG.29



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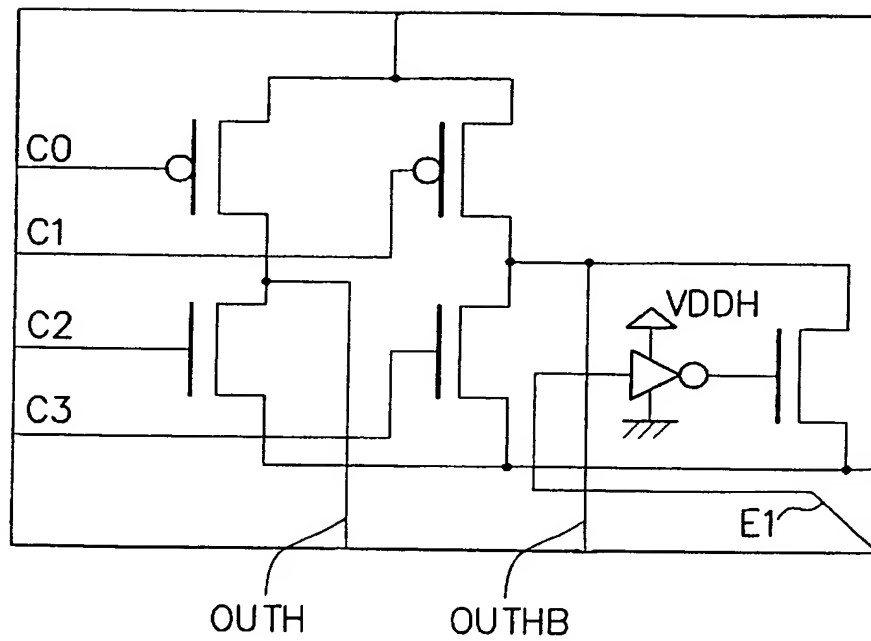
FIG.30



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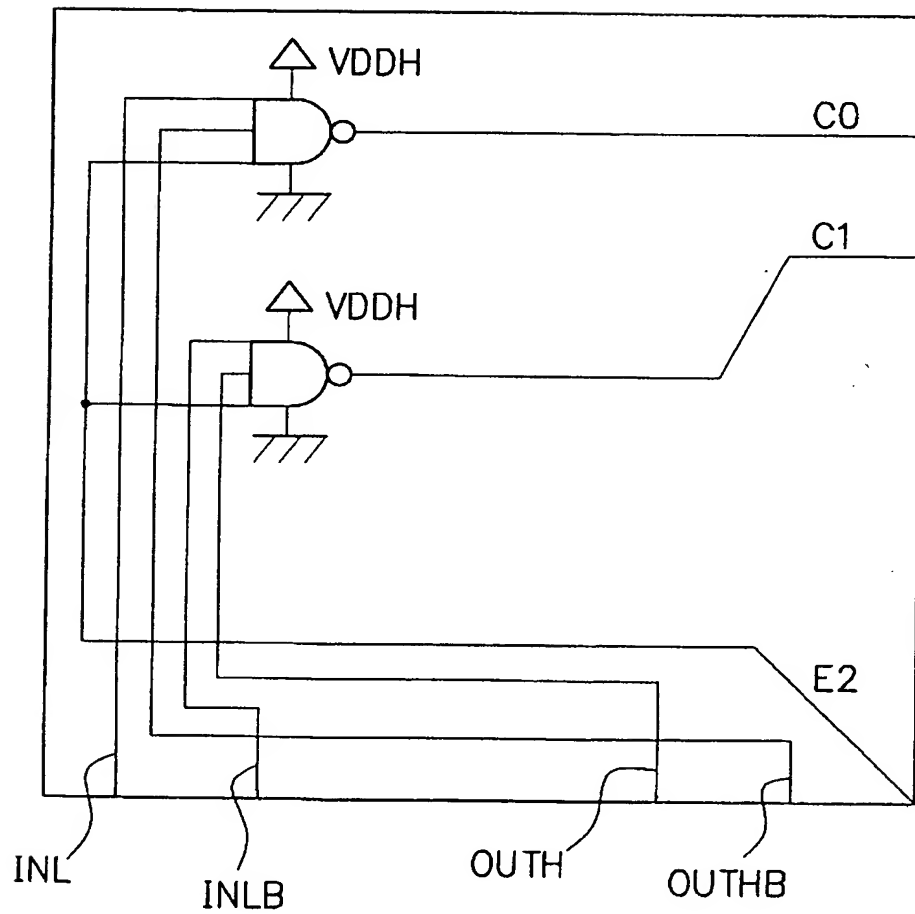
FIG.31



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FIG.32

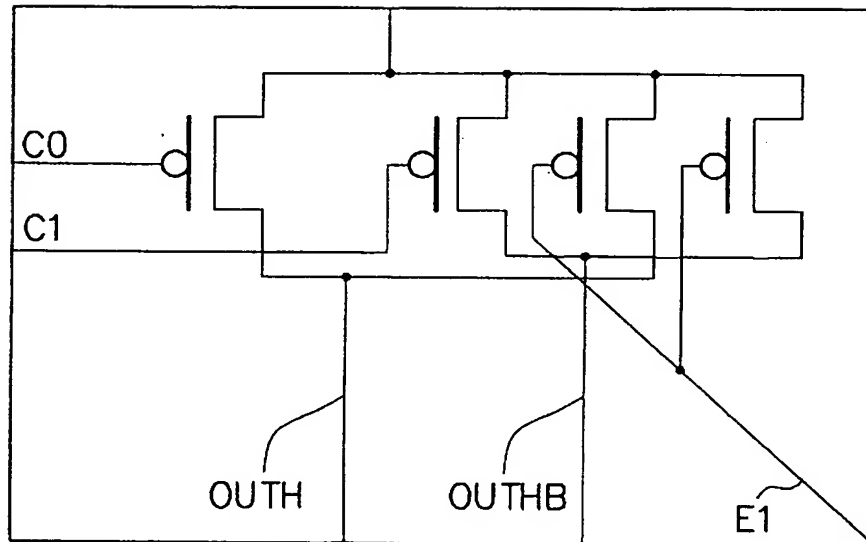




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FIG.33



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FIG.34

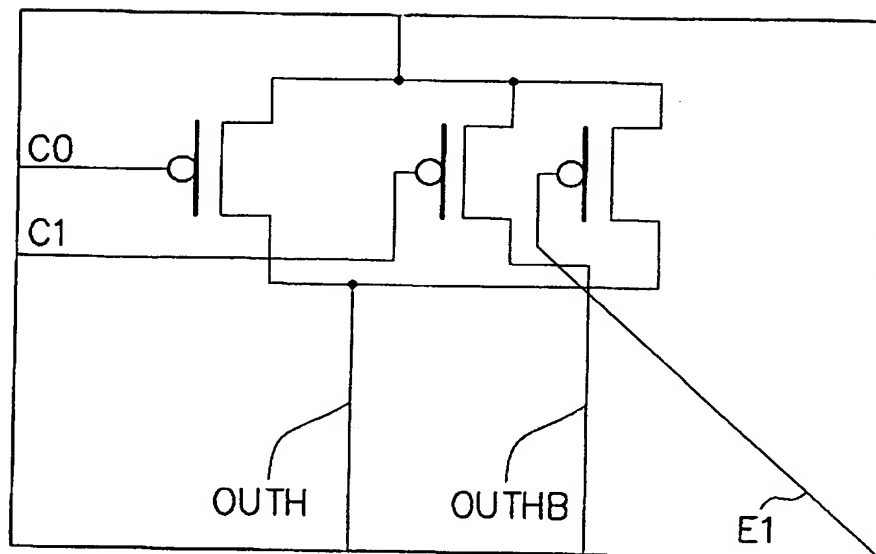


FIG.35

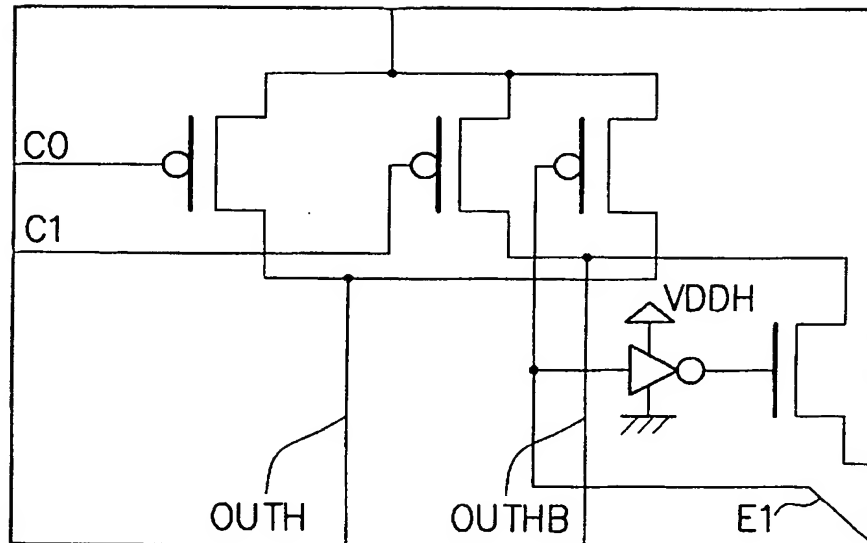
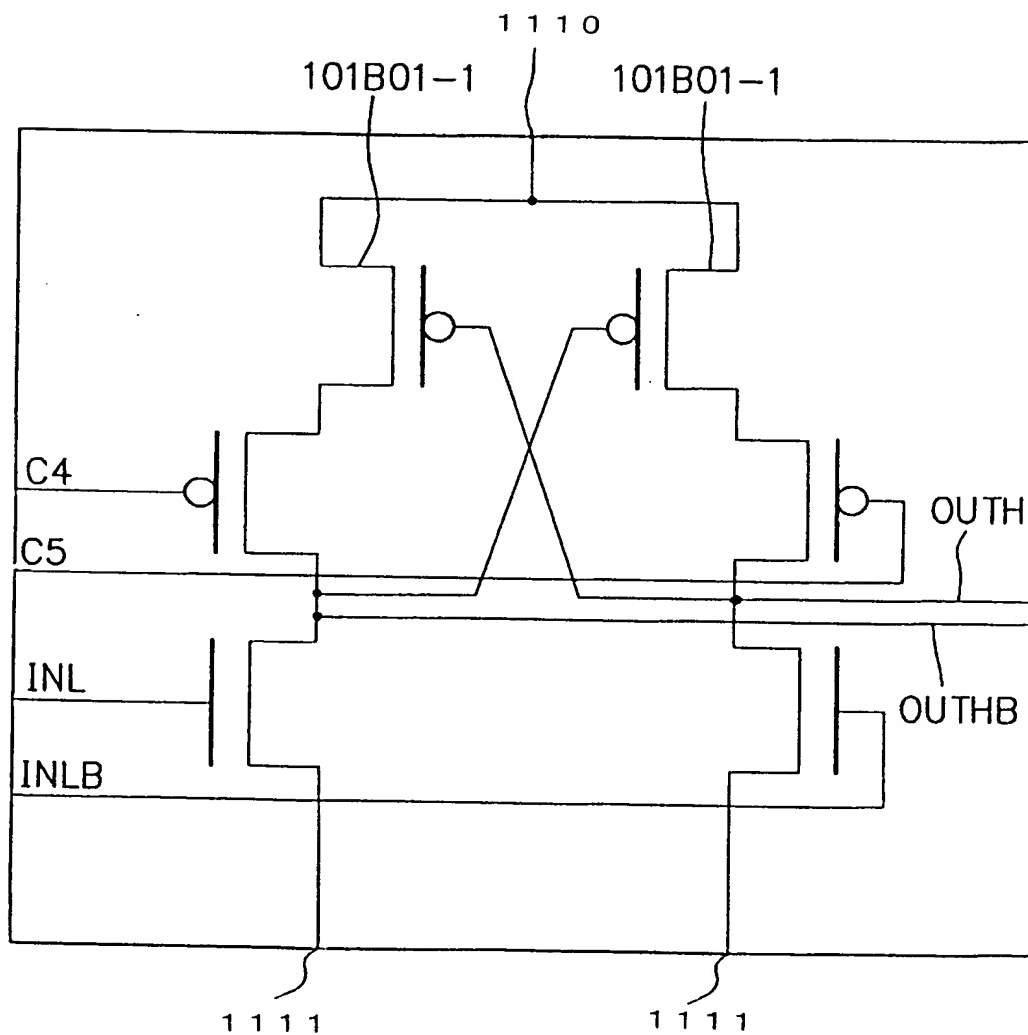




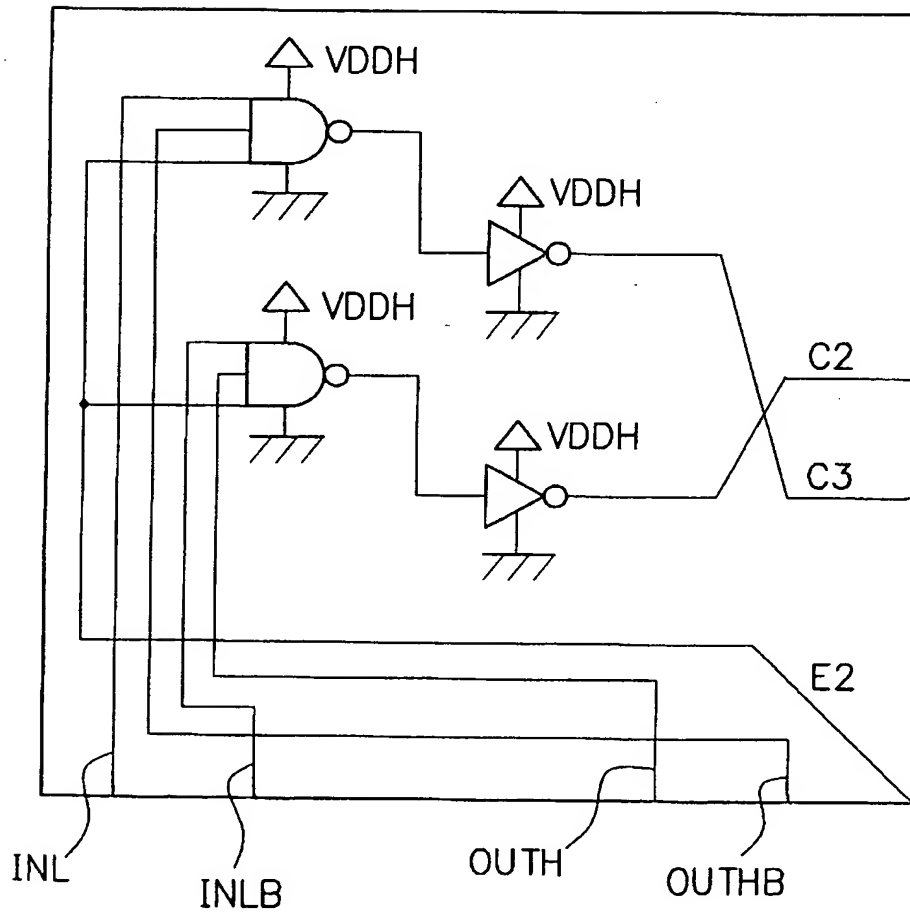
FIG.37



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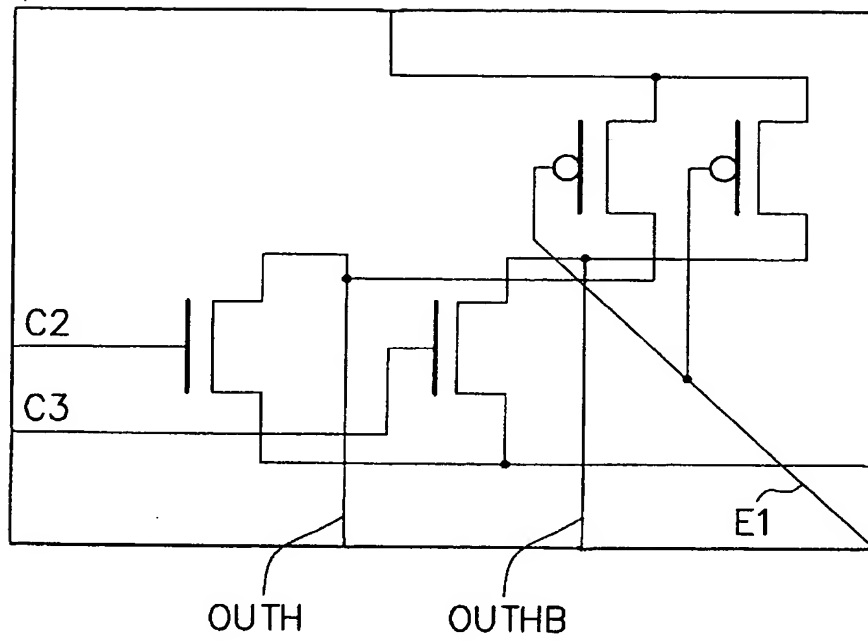
FIG.38



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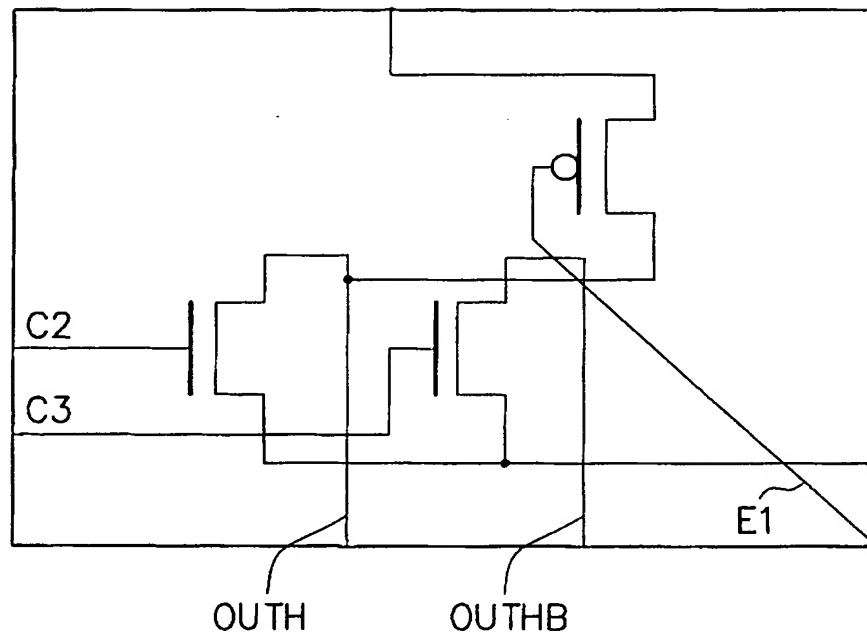
FIG.39



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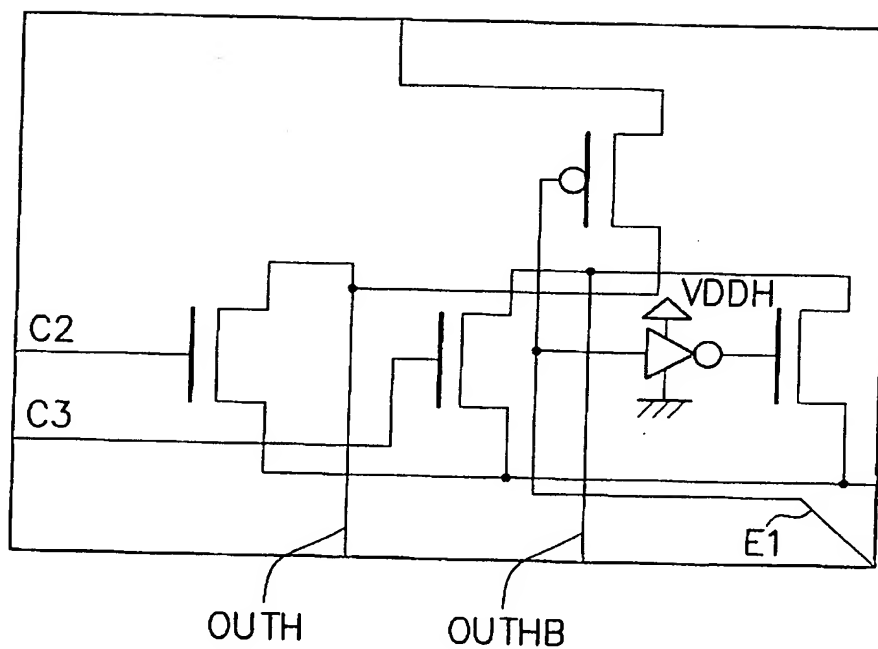
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FIG.40





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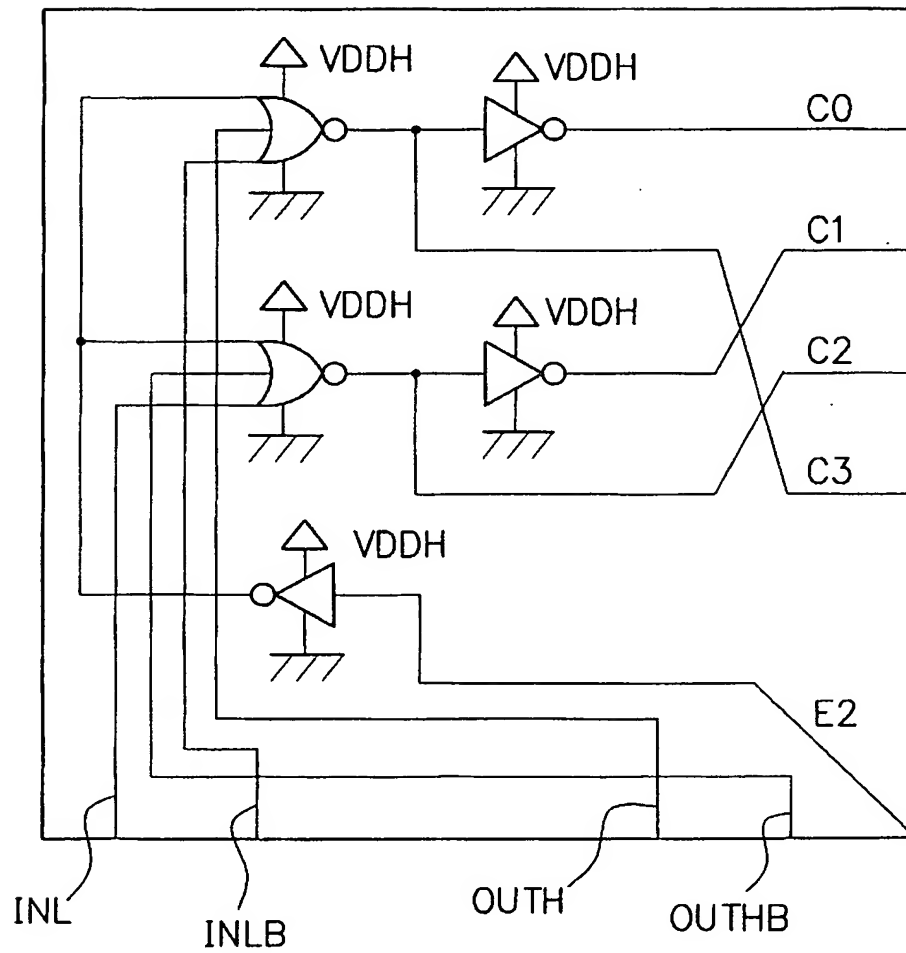


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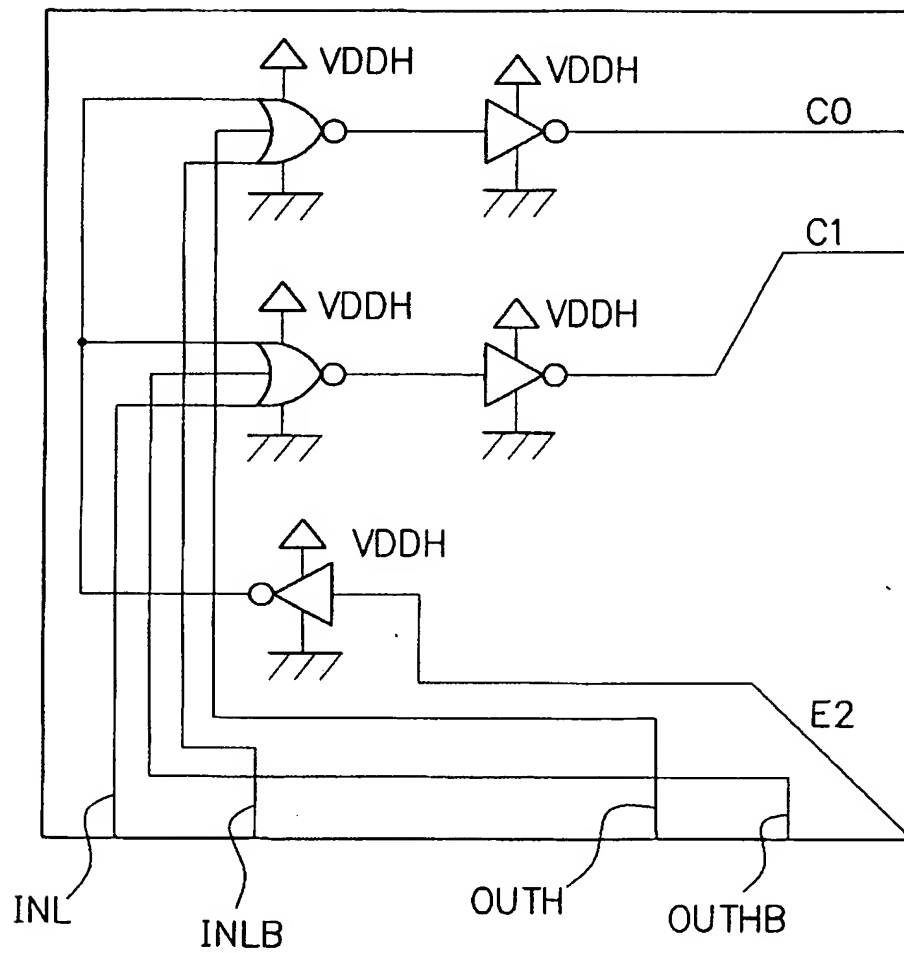
FIG.43



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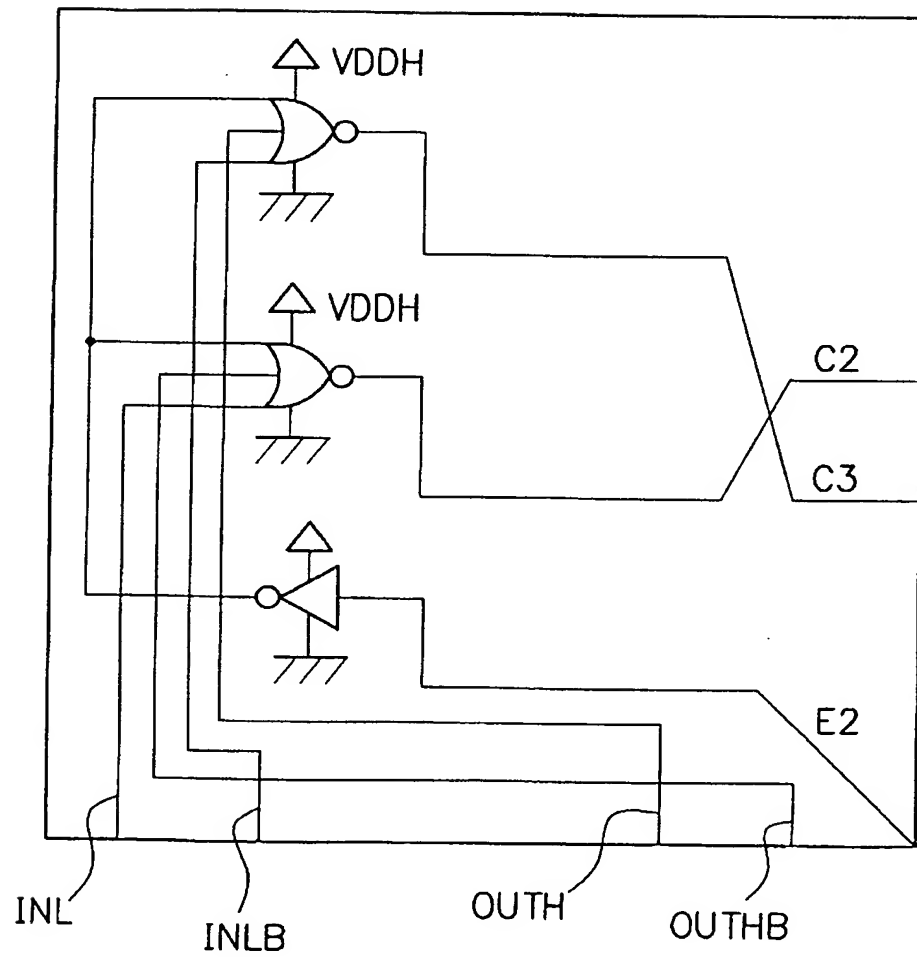
FIG.44



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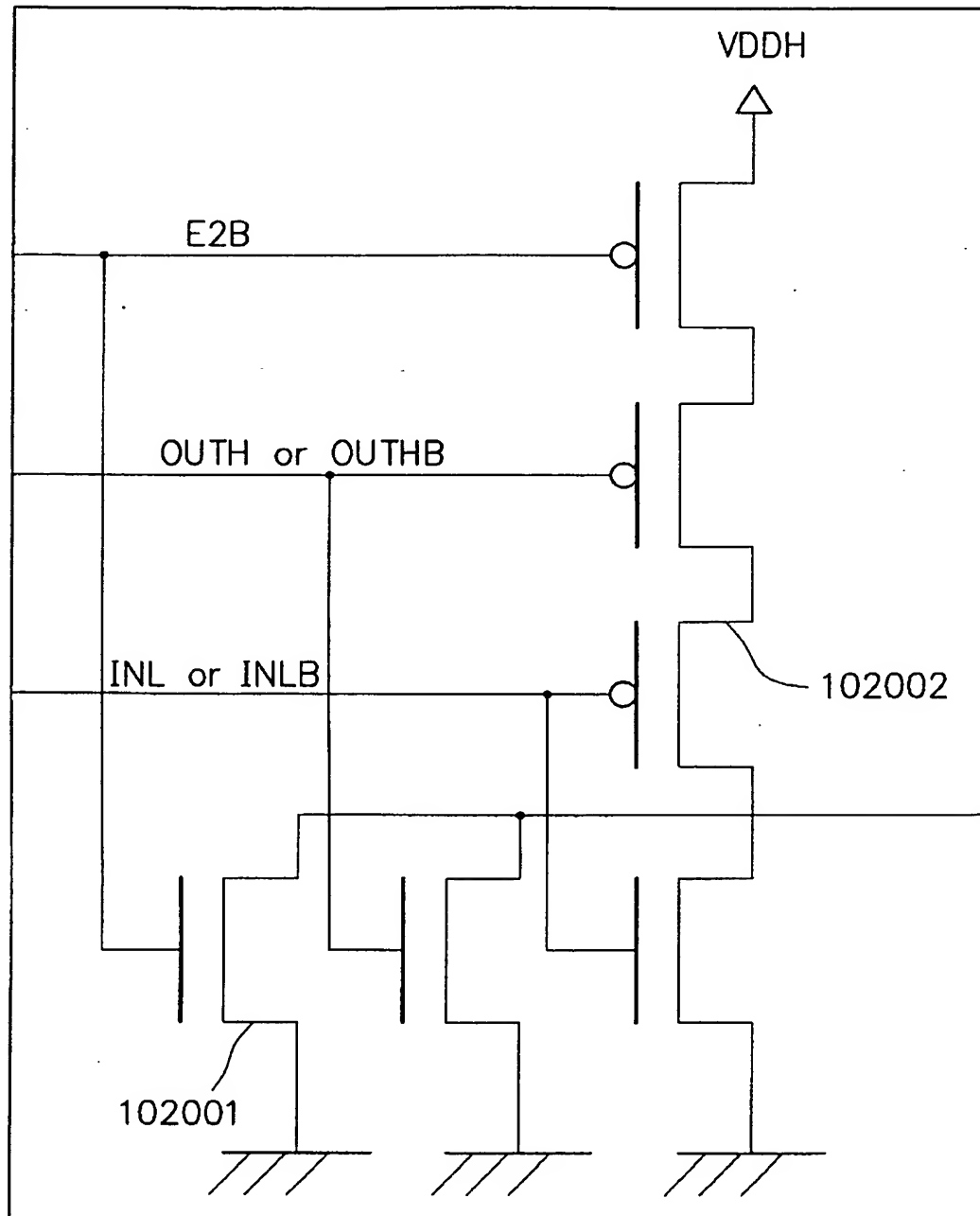
FIG.45



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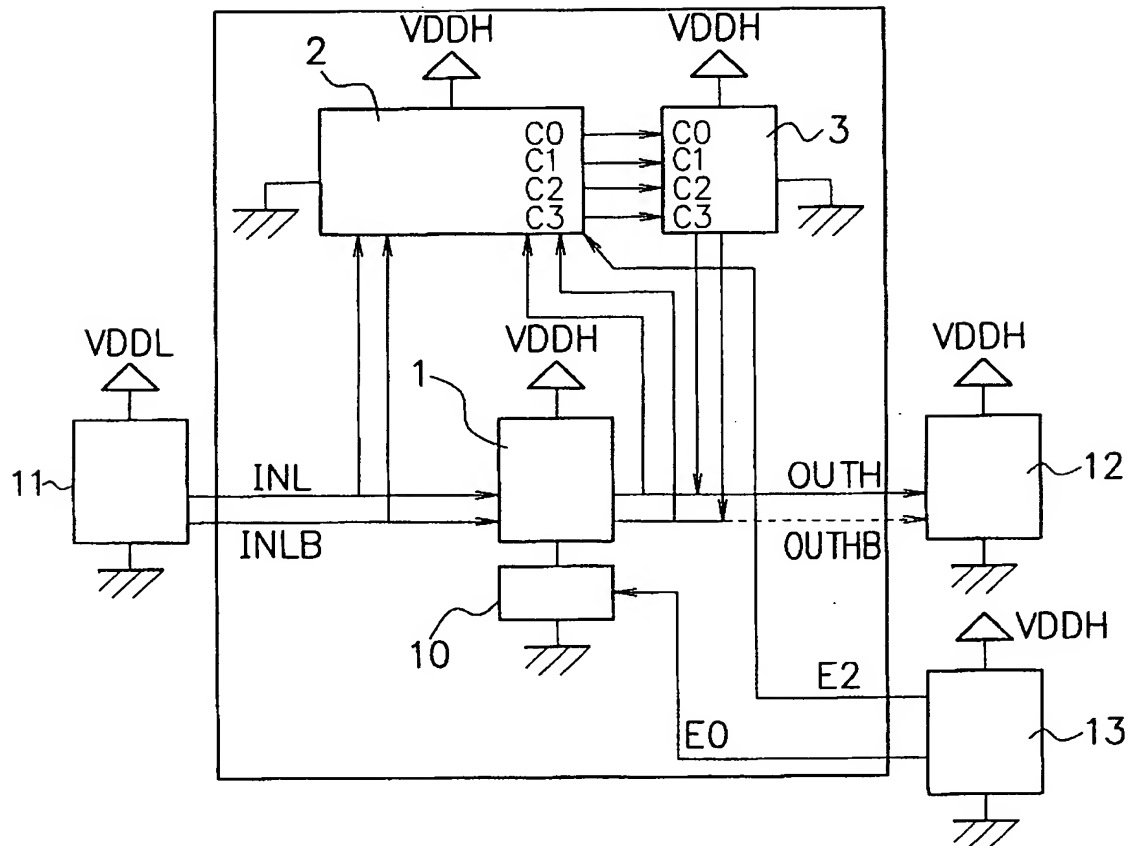
FIG.46



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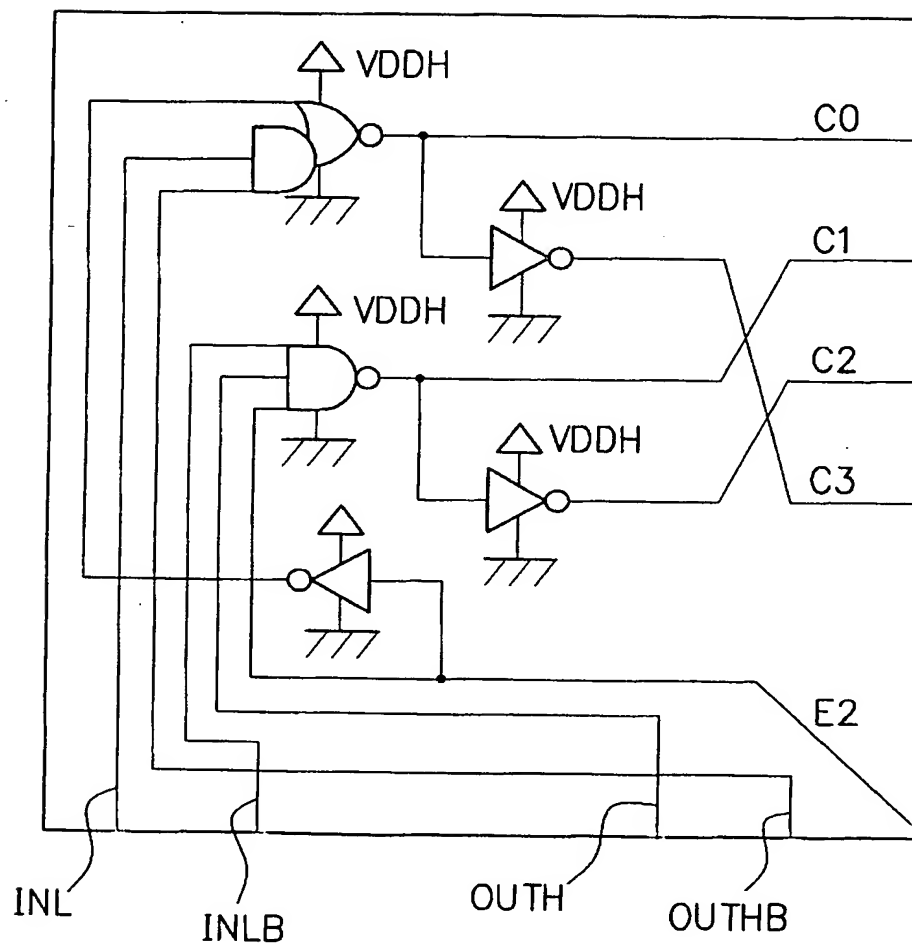
FIG.47



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FIG.48

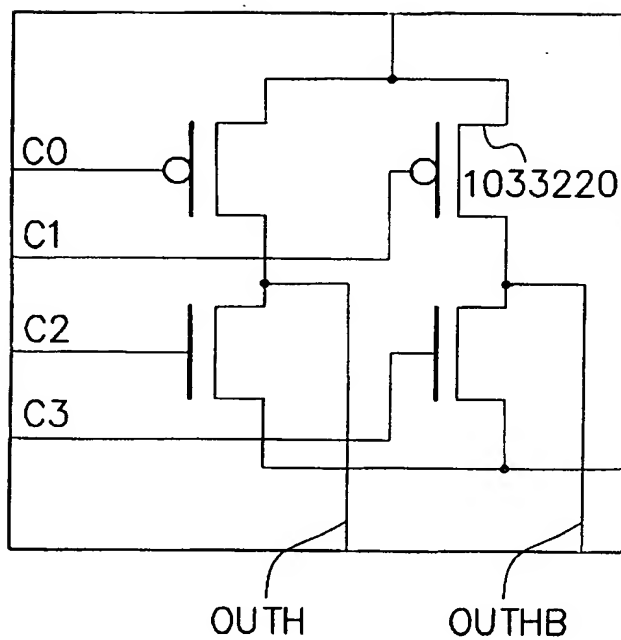




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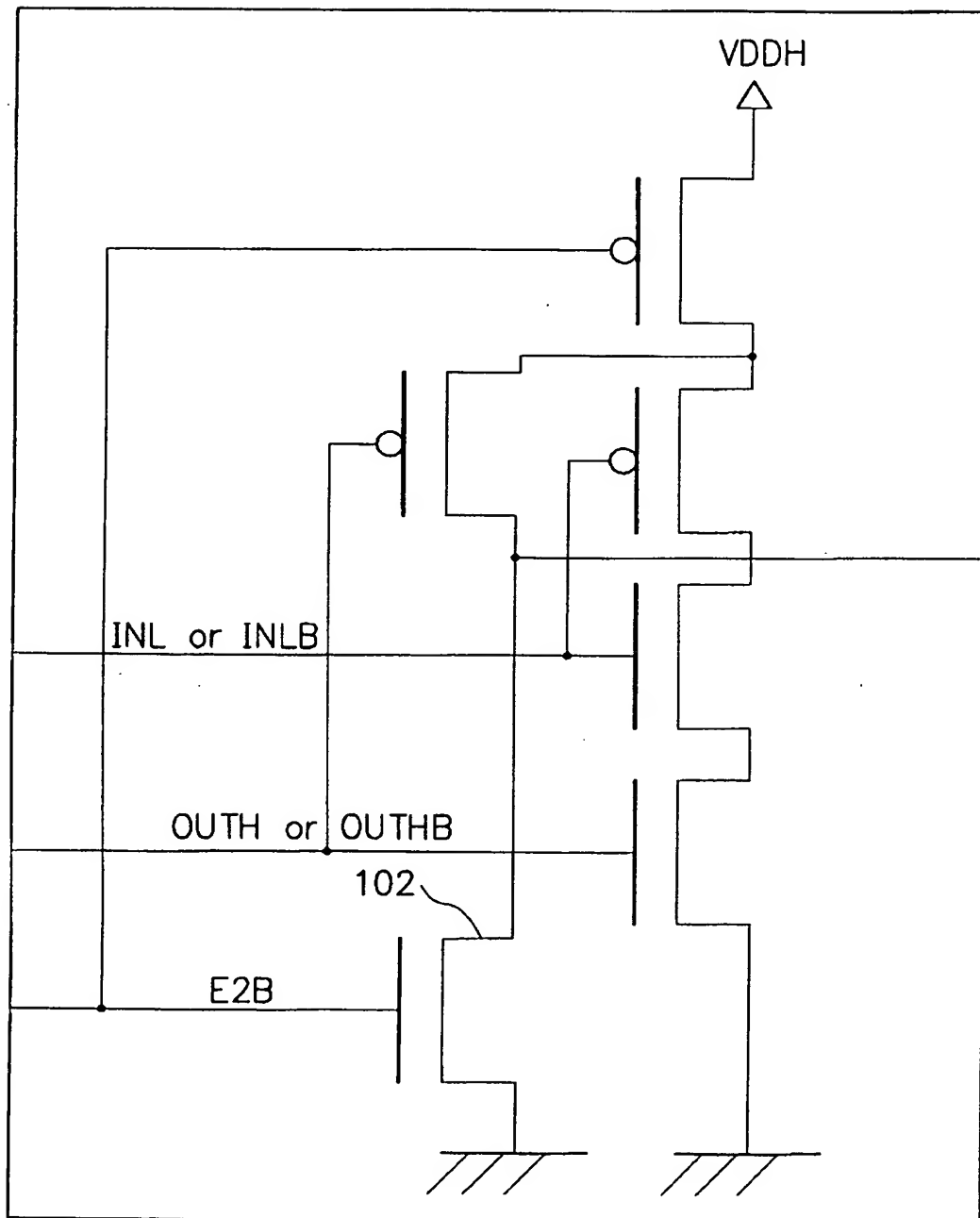
FIG.49



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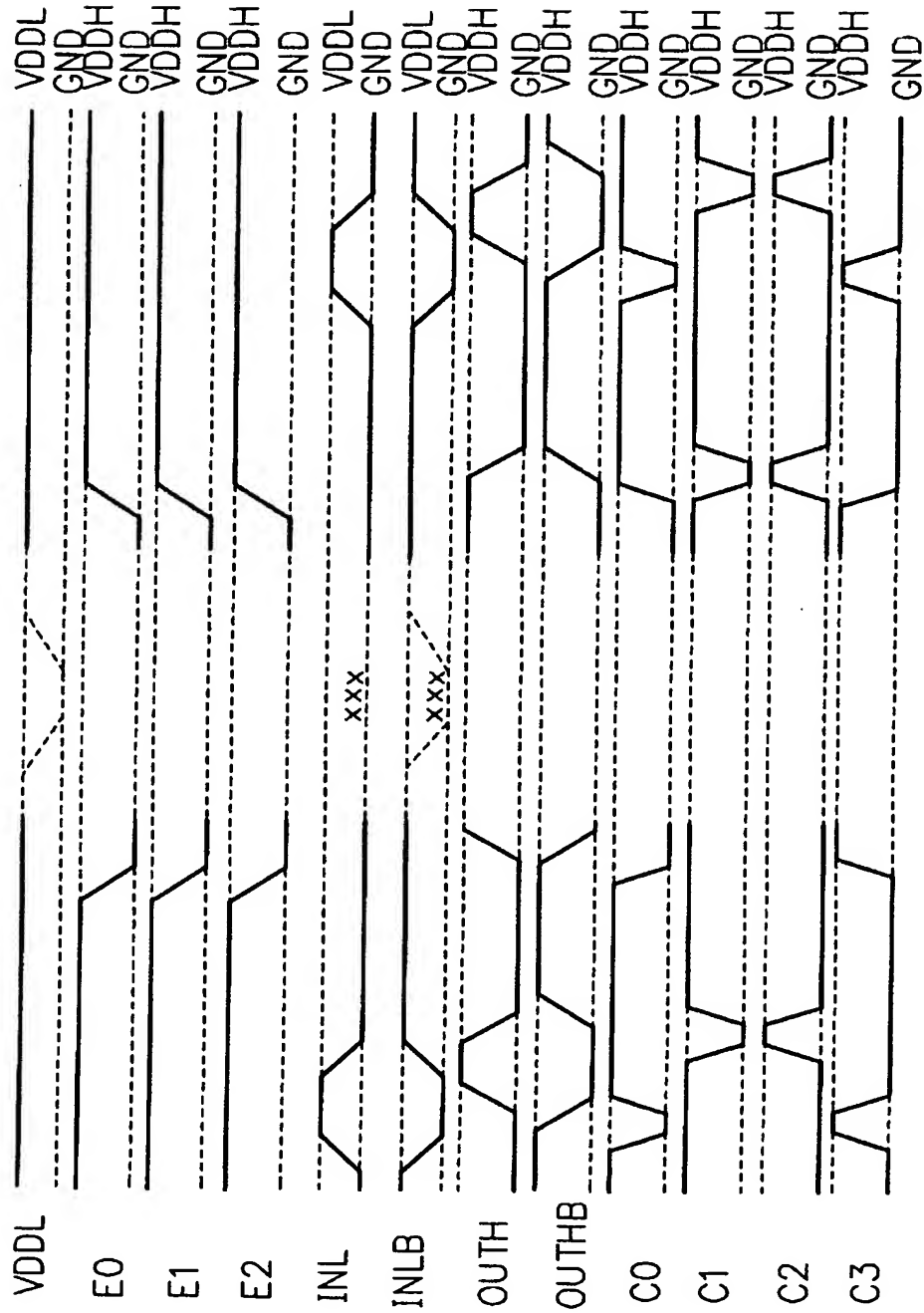
FIG.50



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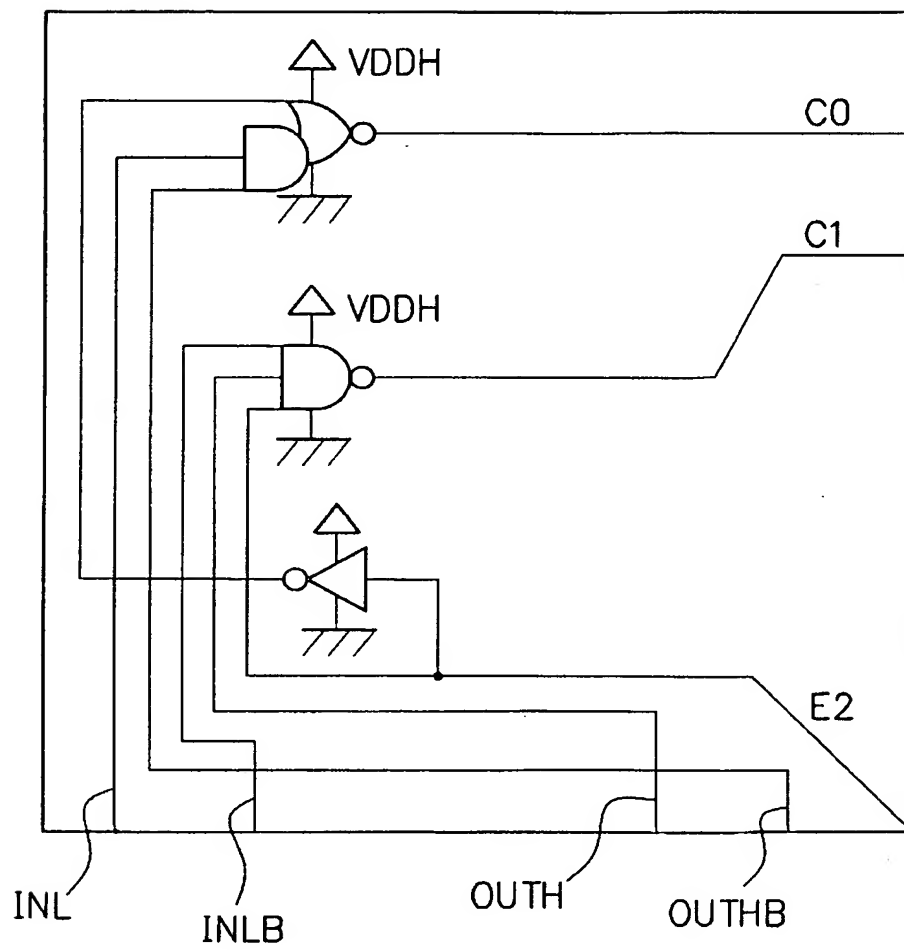
FIG.51



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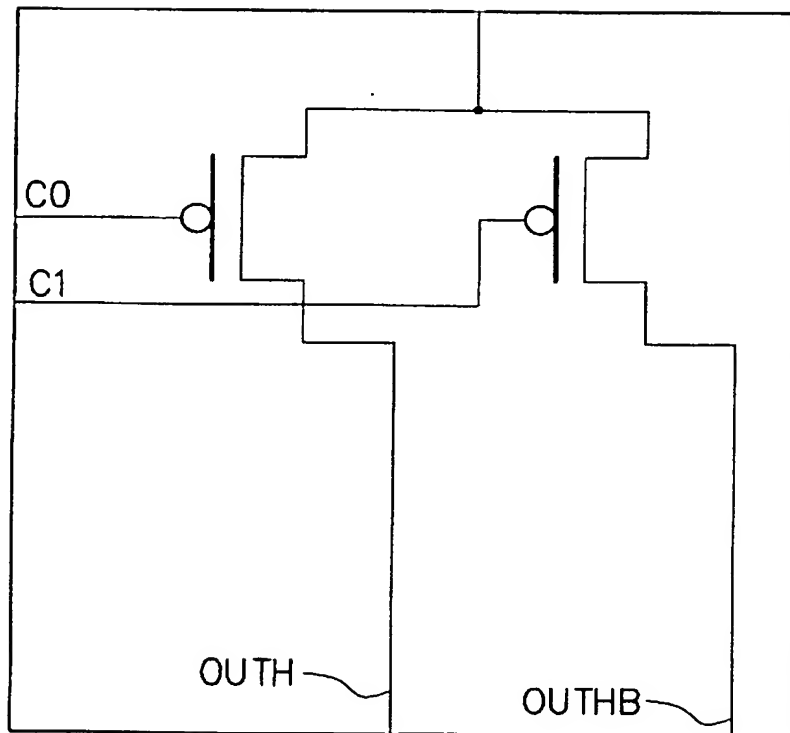
FIG.52



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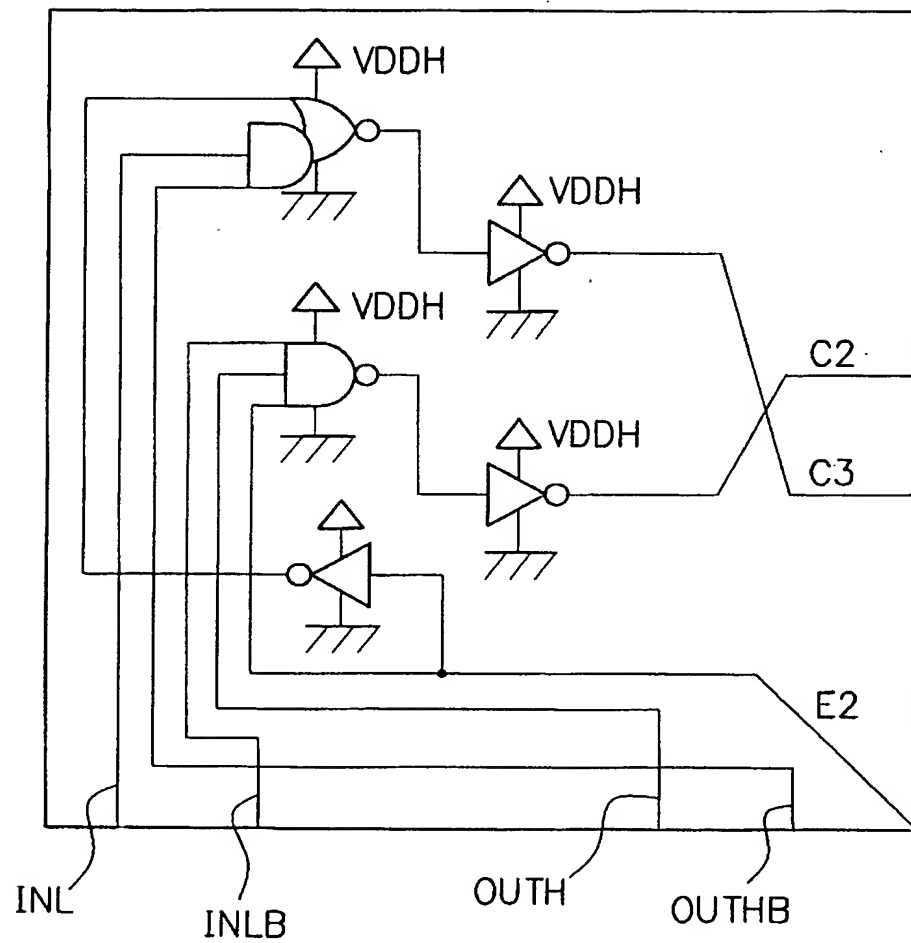
FIG.53



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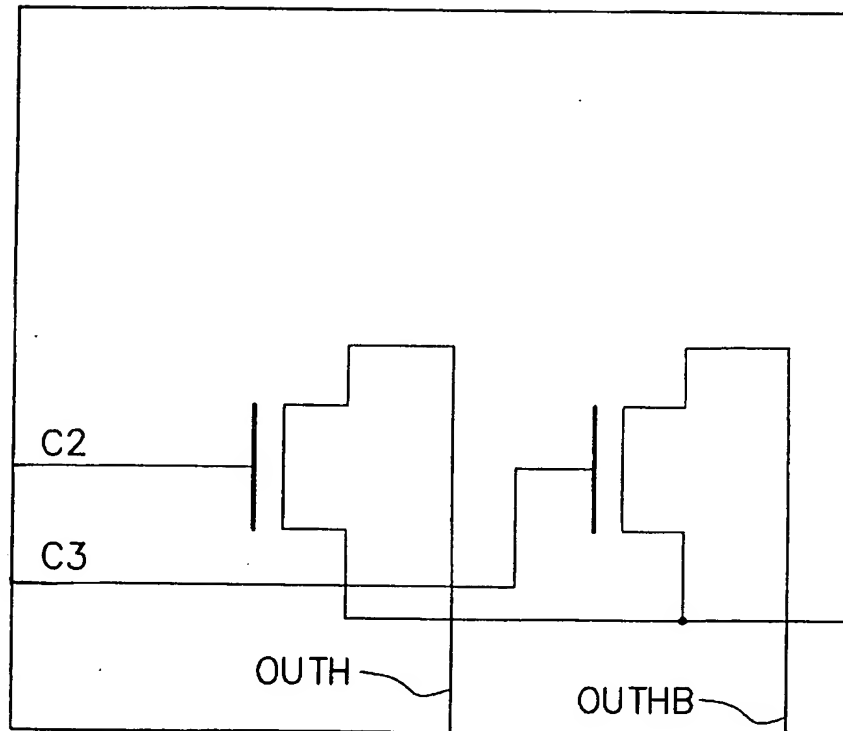
FIG.54



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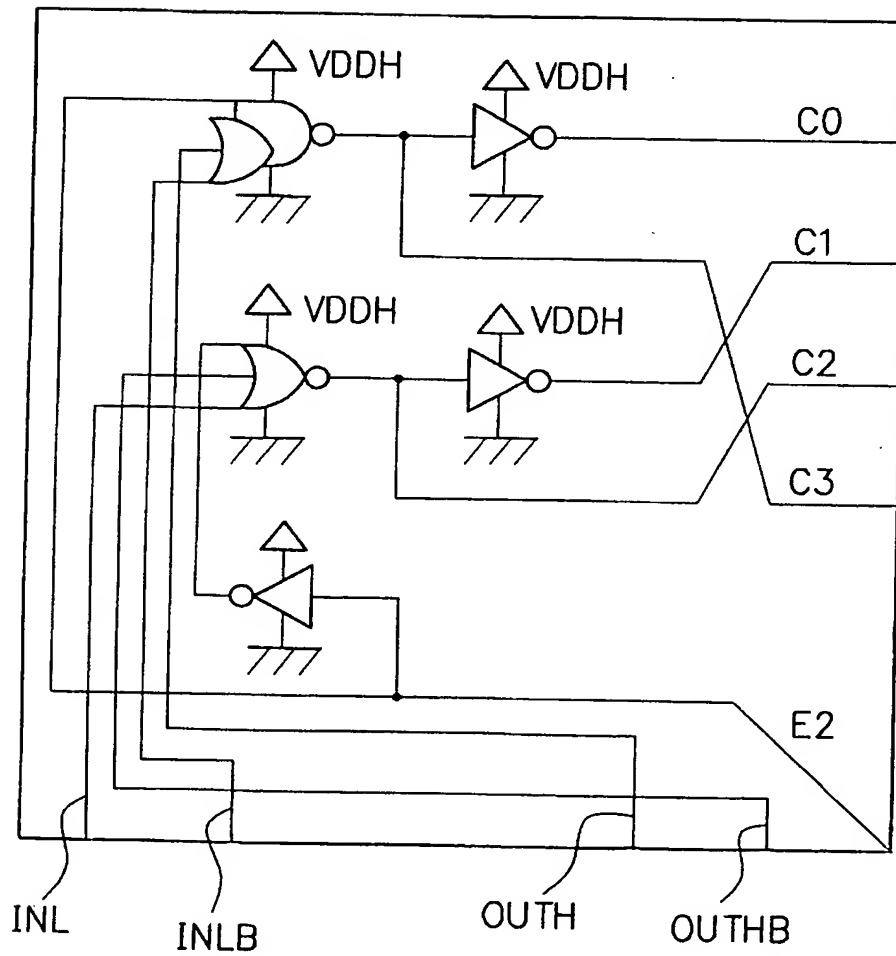
FIG.55



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FIG.56

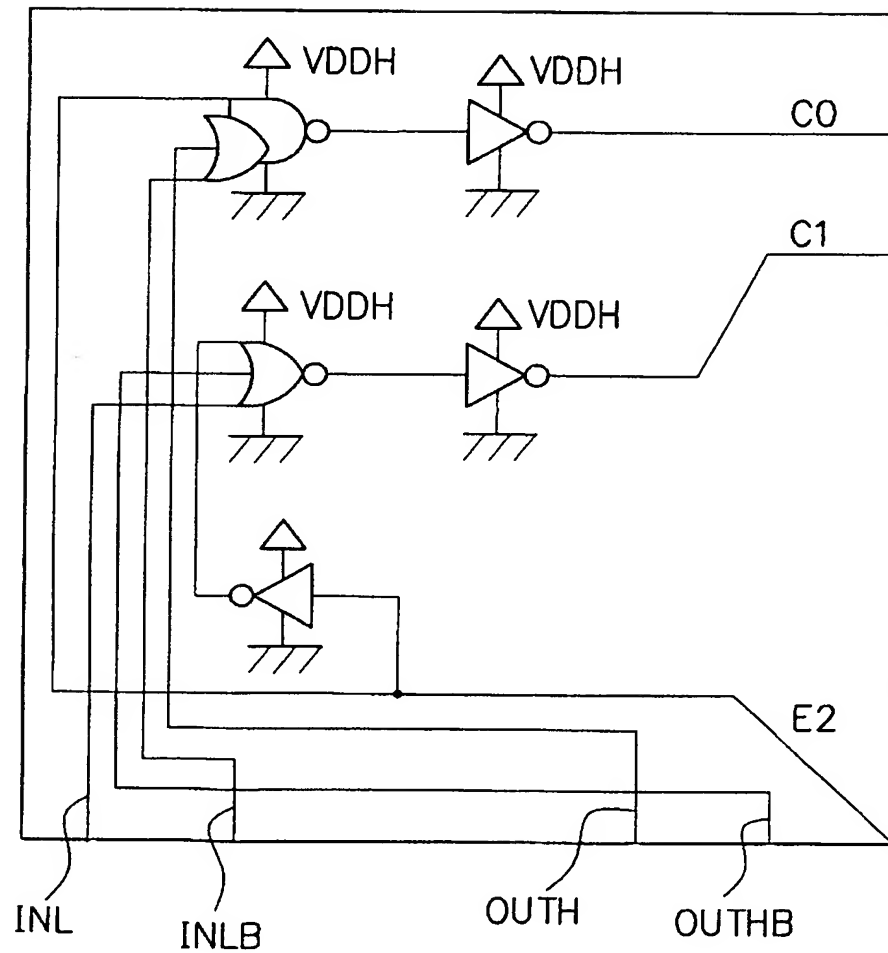




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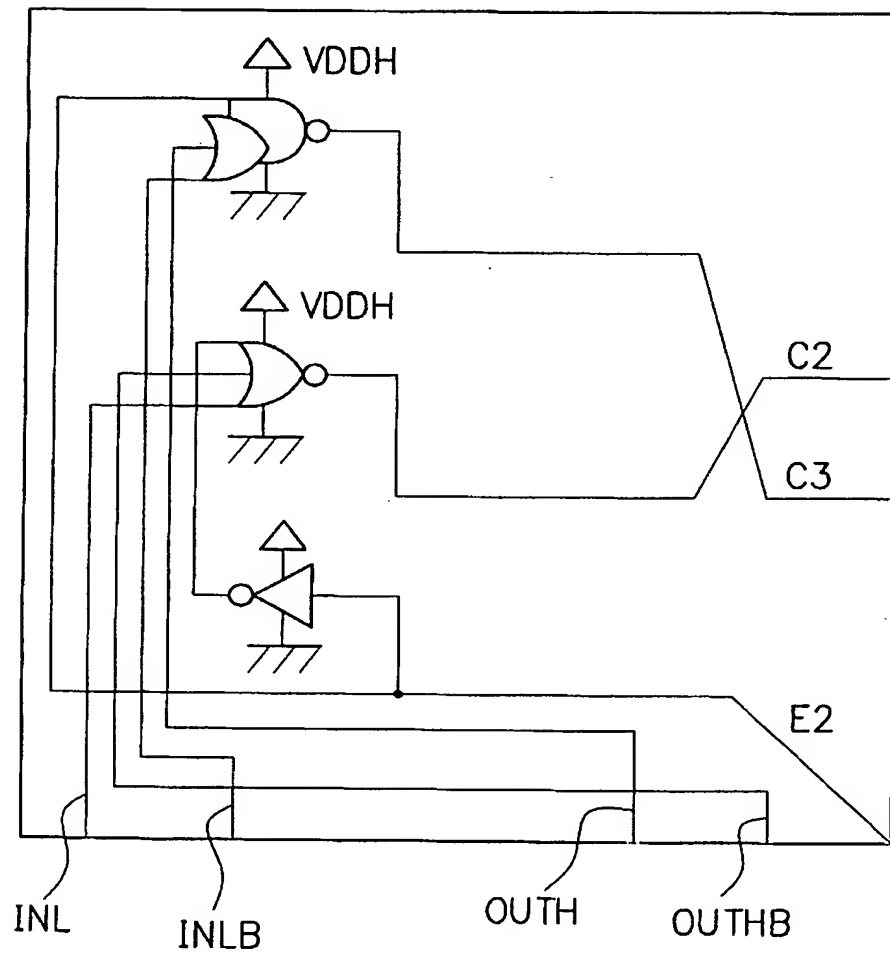
FIG.57



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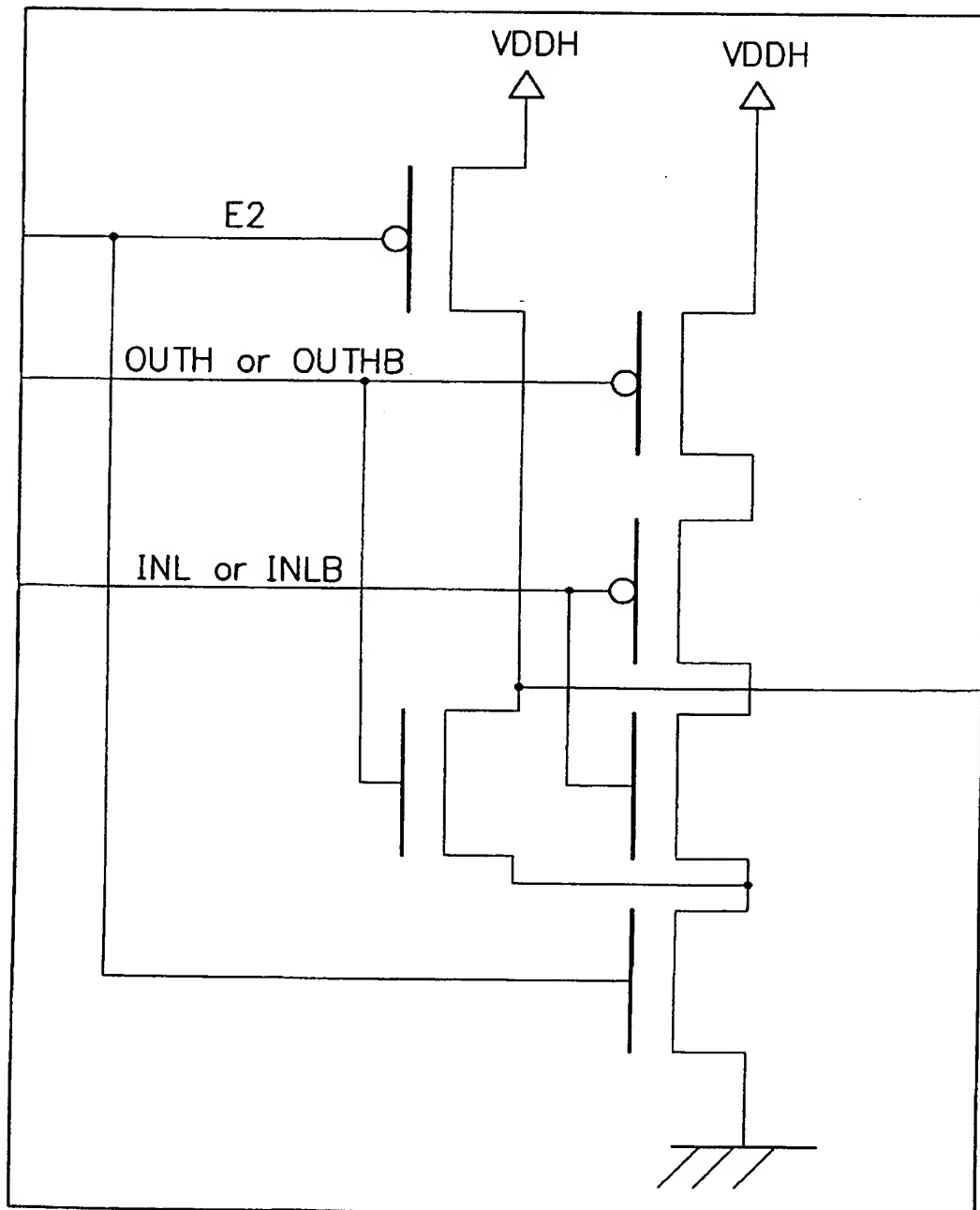
FIG.58



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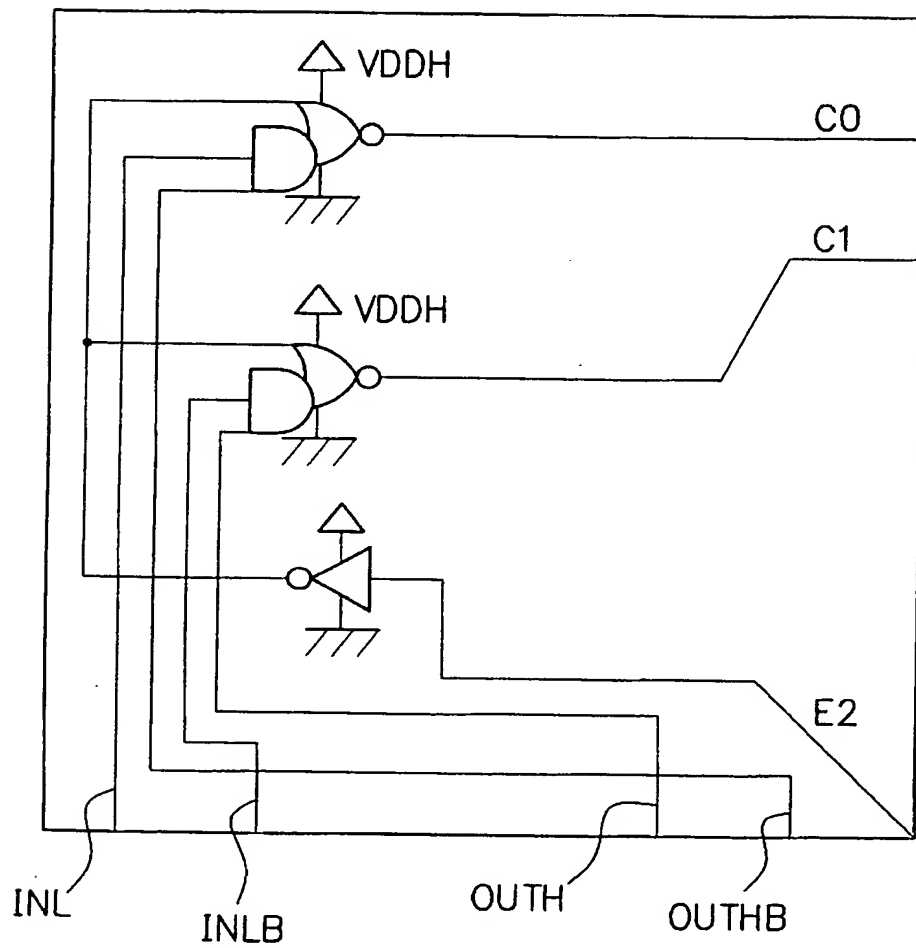
FIG.59



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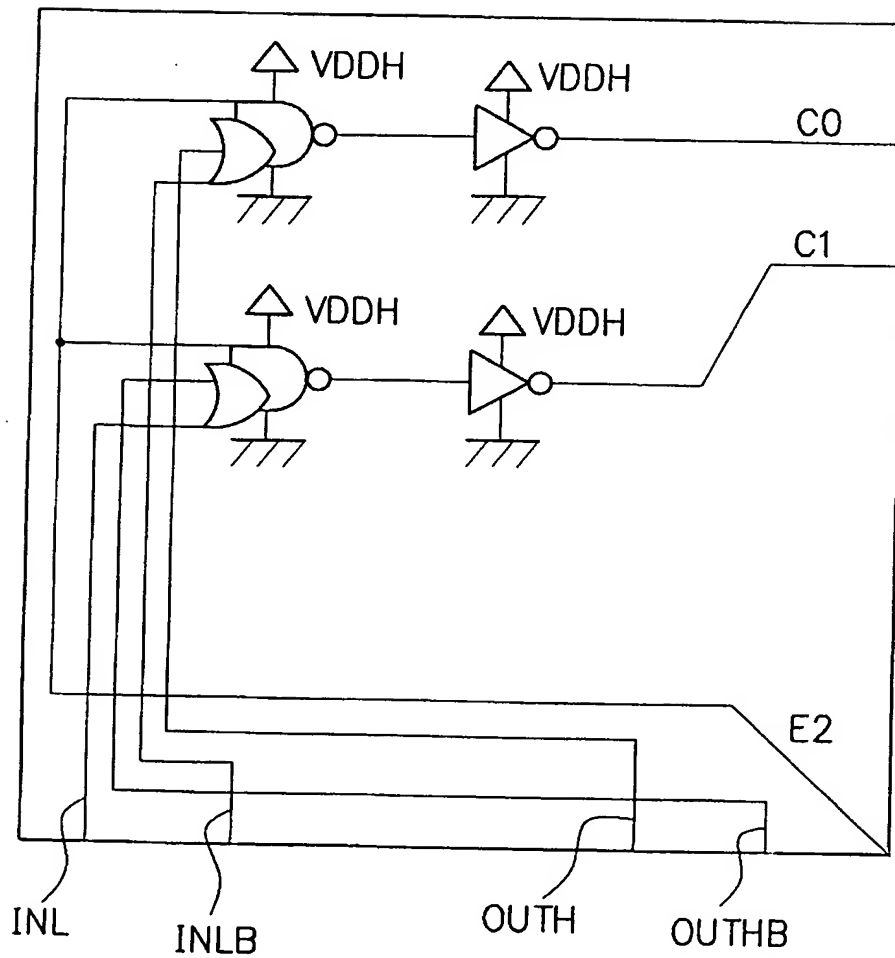
FIG.60



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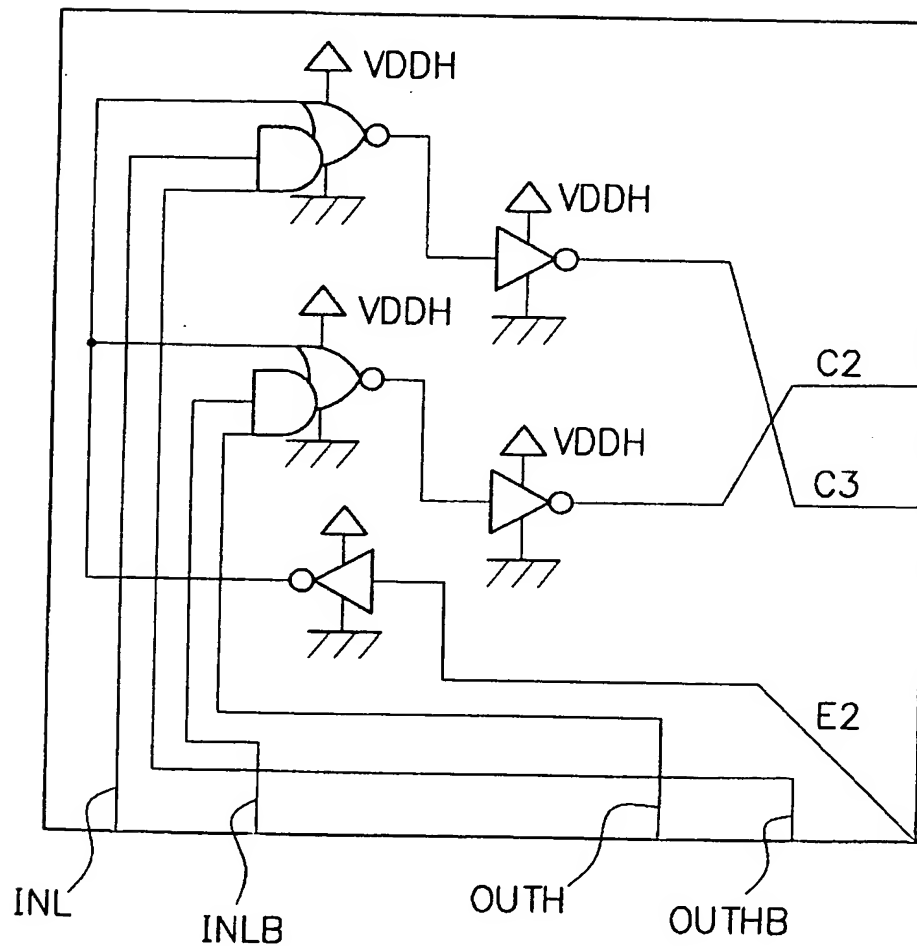
FIG.61



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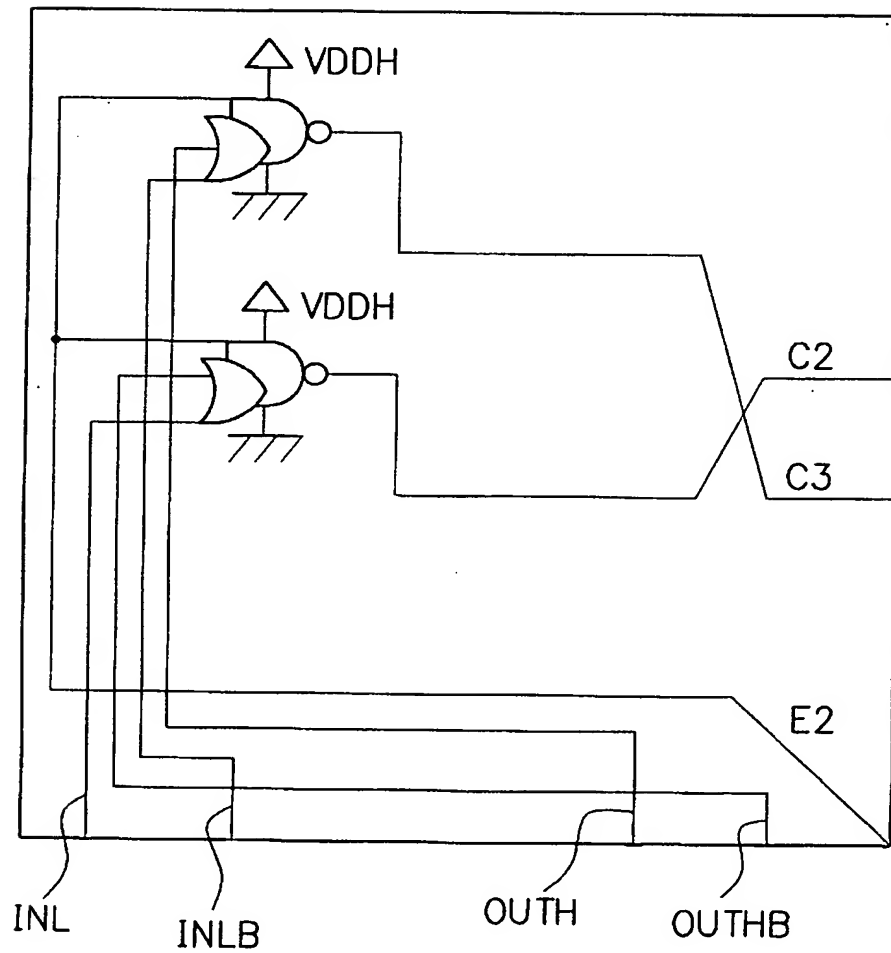
FIG.62



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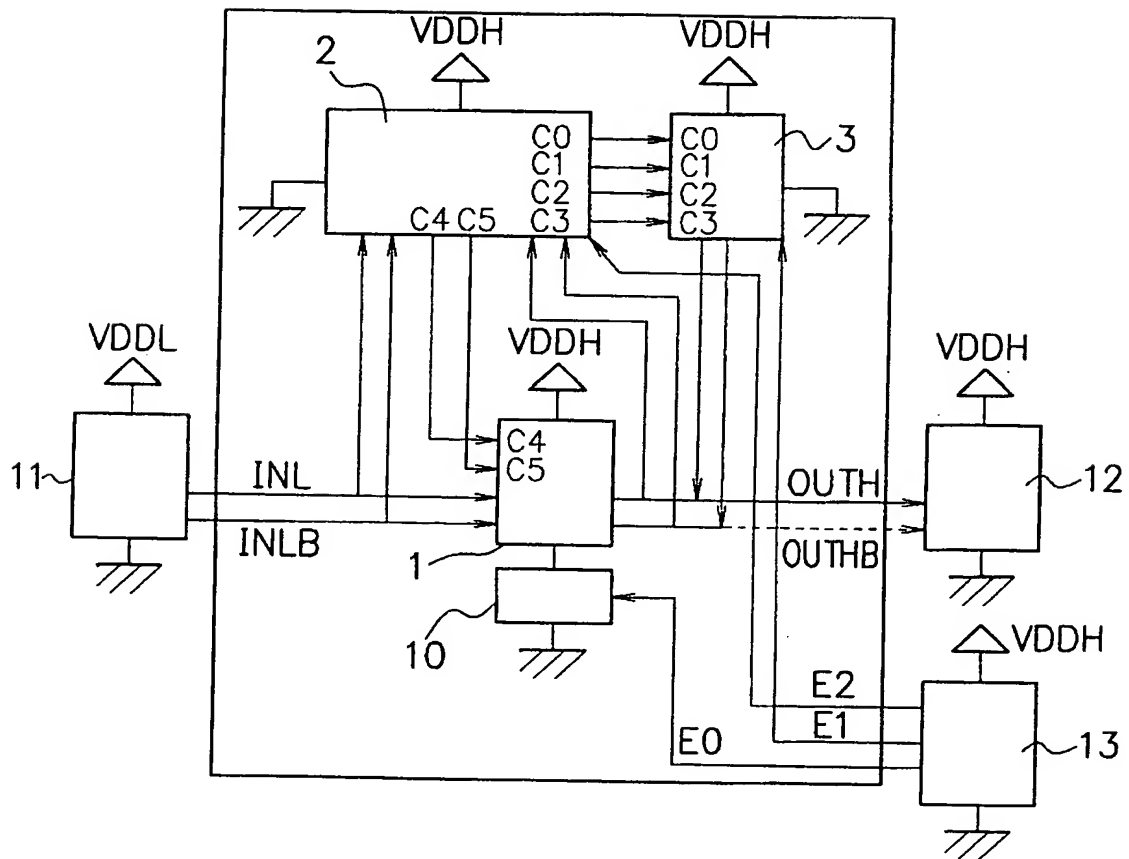
FIG.63



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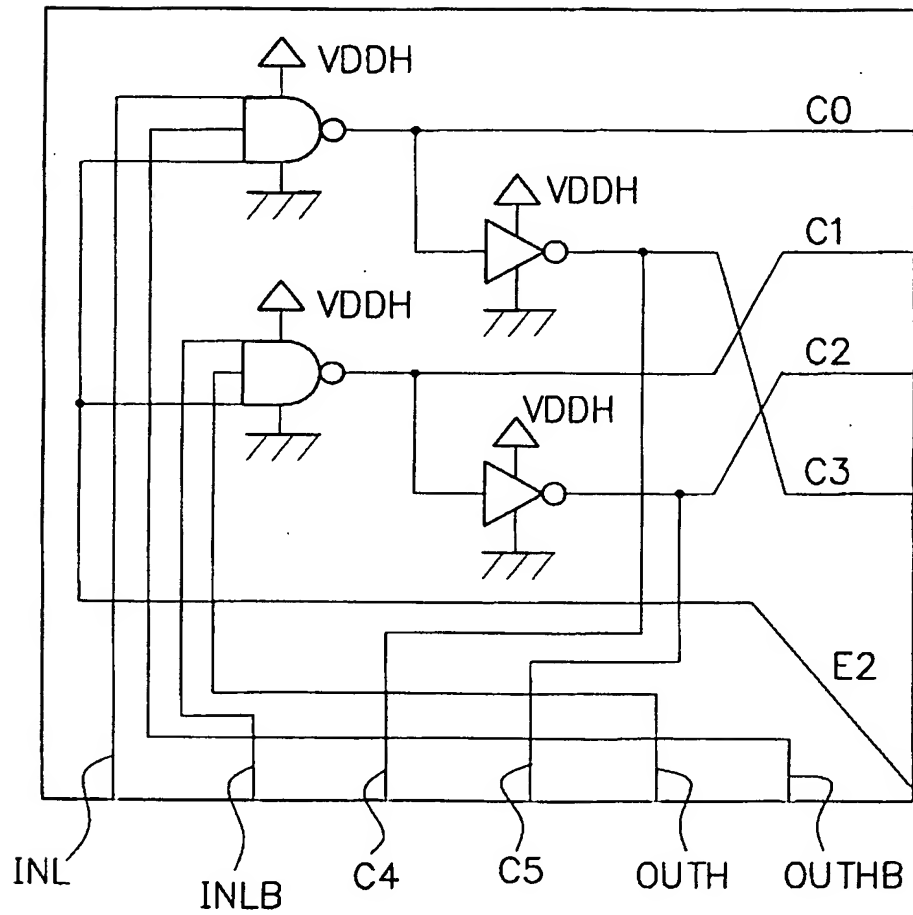
FIG.64





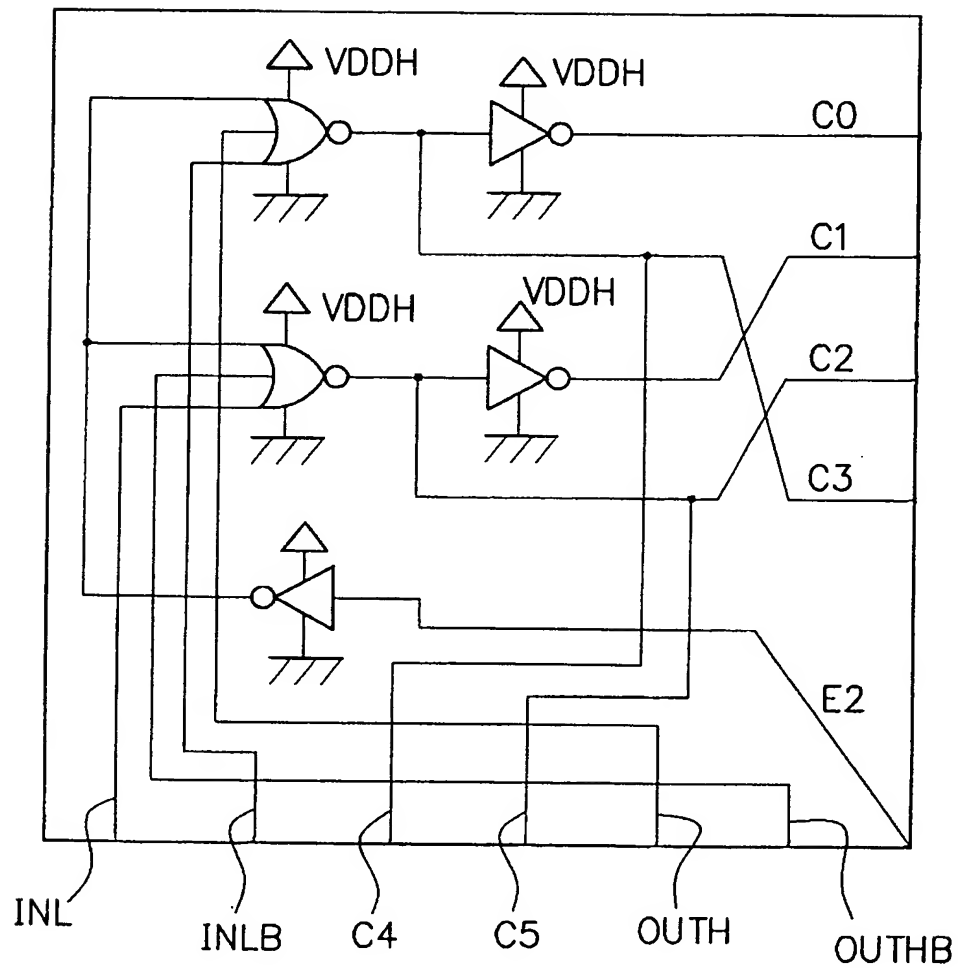
The diagram shows a complex circuit with multiple inputs and outputs. Inputs on the left are labeled INL, INLB, C4, and C5. Outputs on the right are labeled OUTH and OUTHB. The circuit features a central cross-coupled section with two vertical lines labeled 101B01-1. The bottom of the circuit is connected to a common ground line.

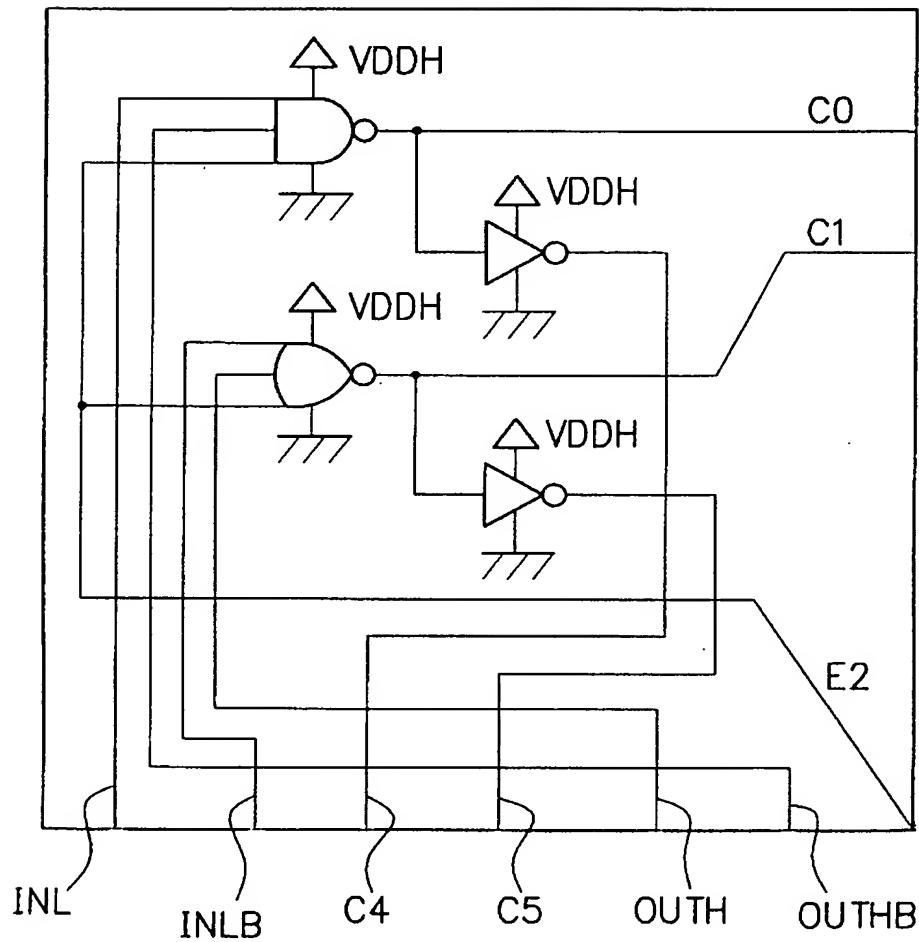
FIG.66



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FIG.67

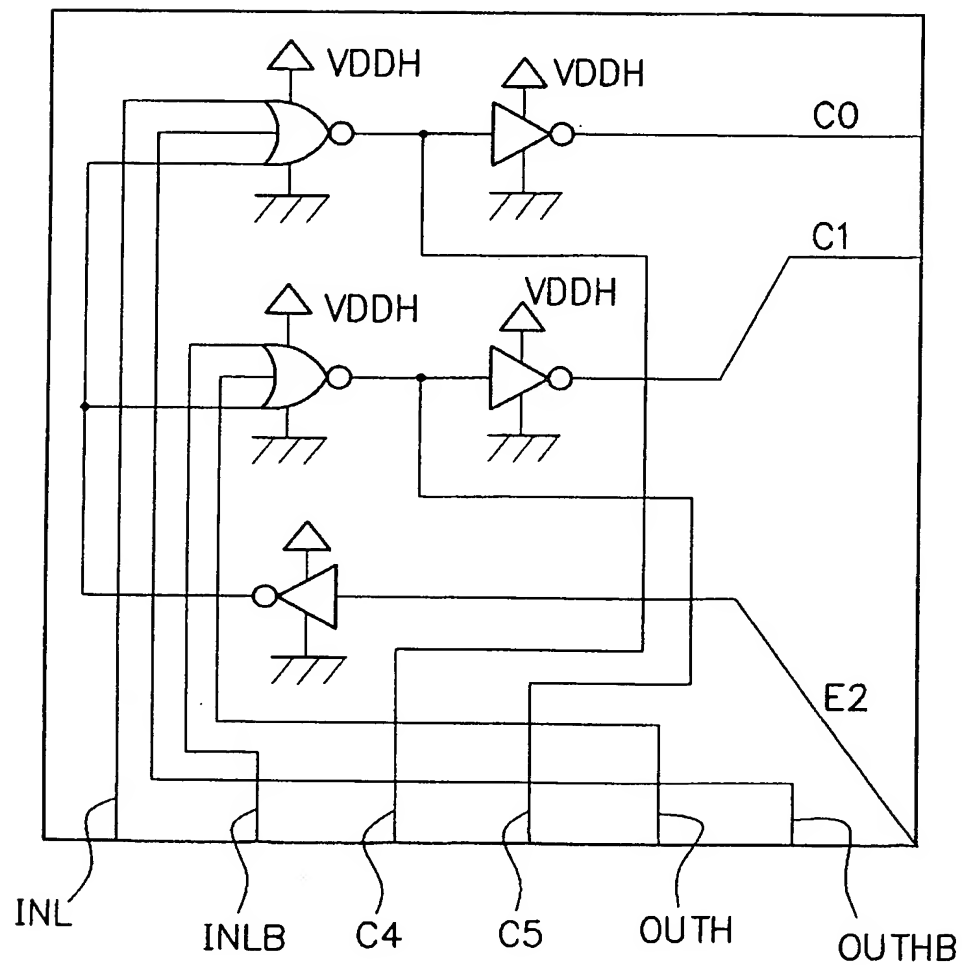




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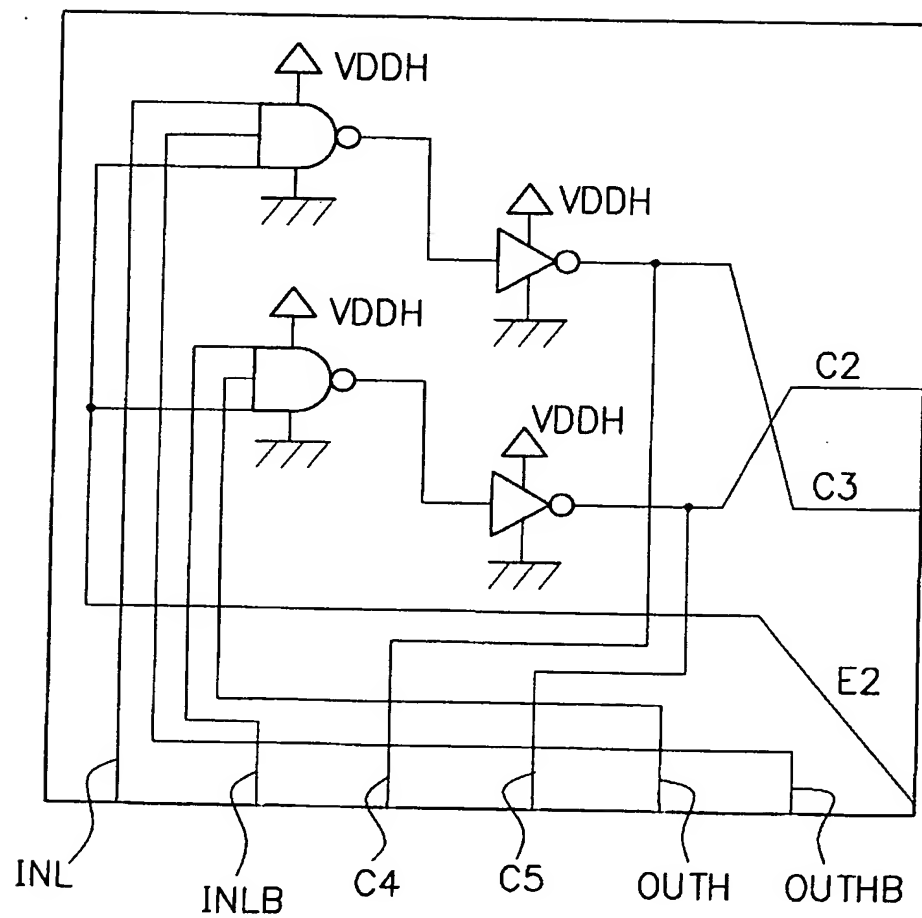
FIG.69



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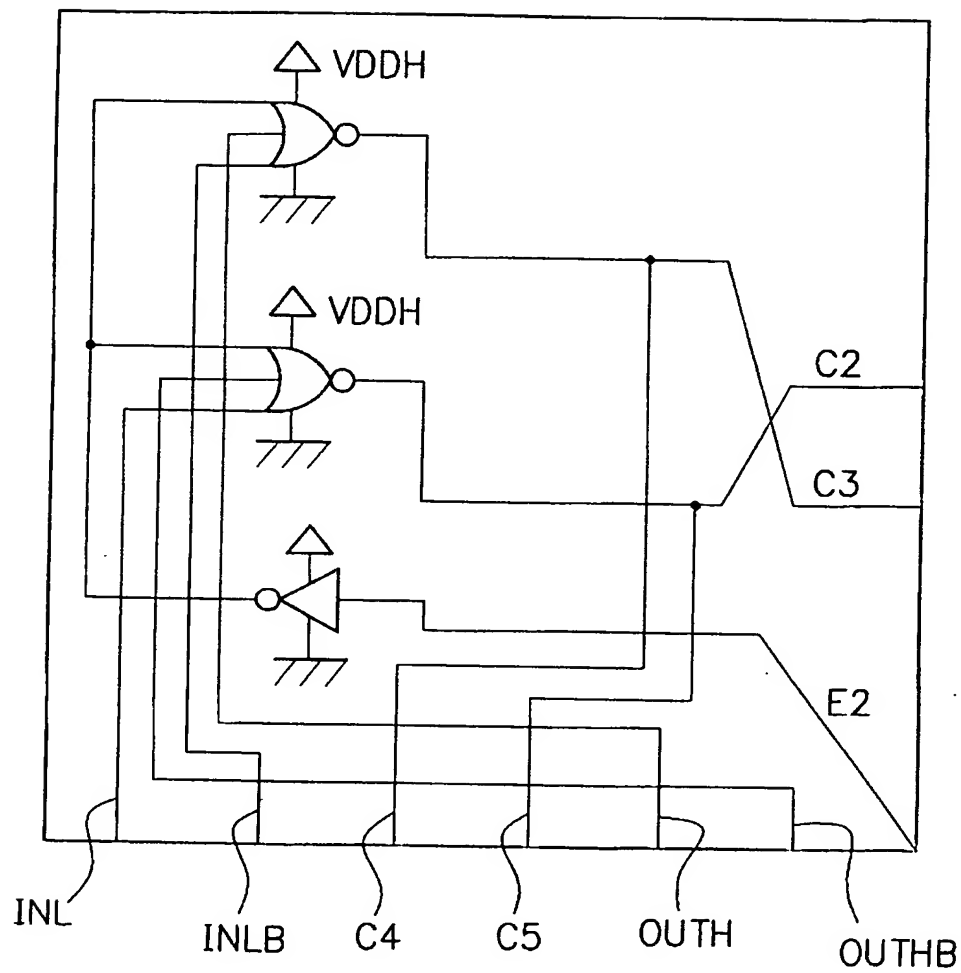
FIG. 70



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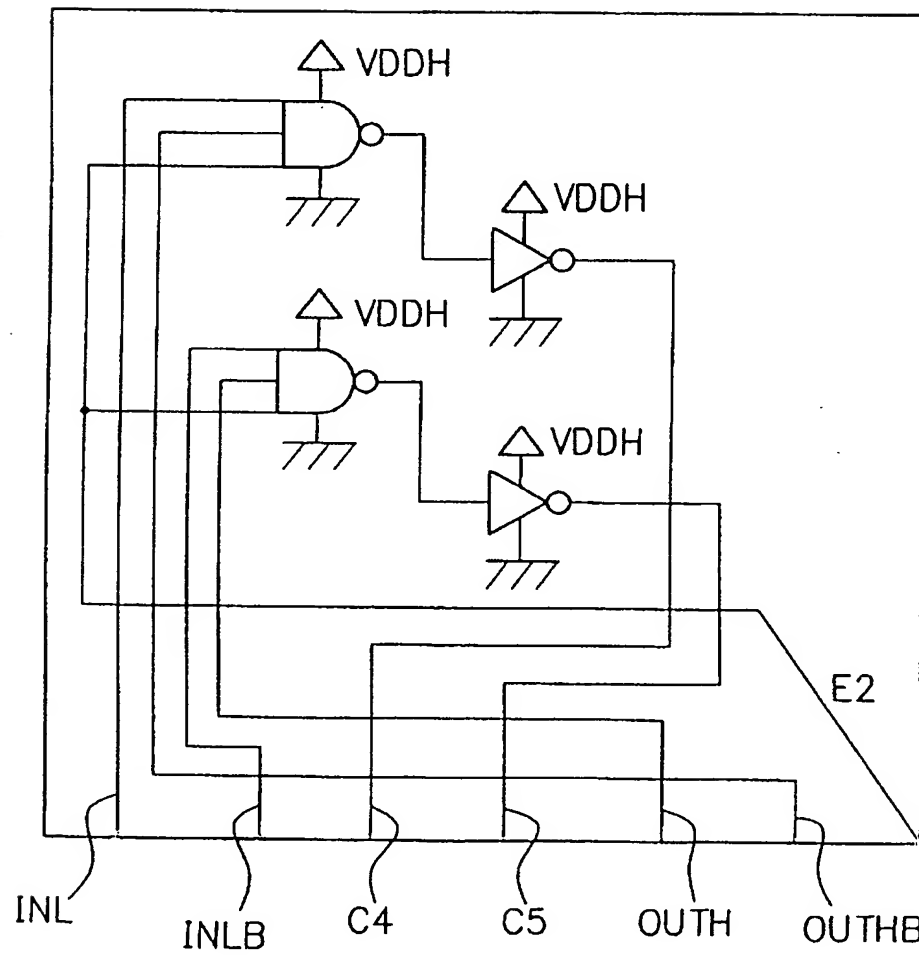
FIG.71



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FIG. 72

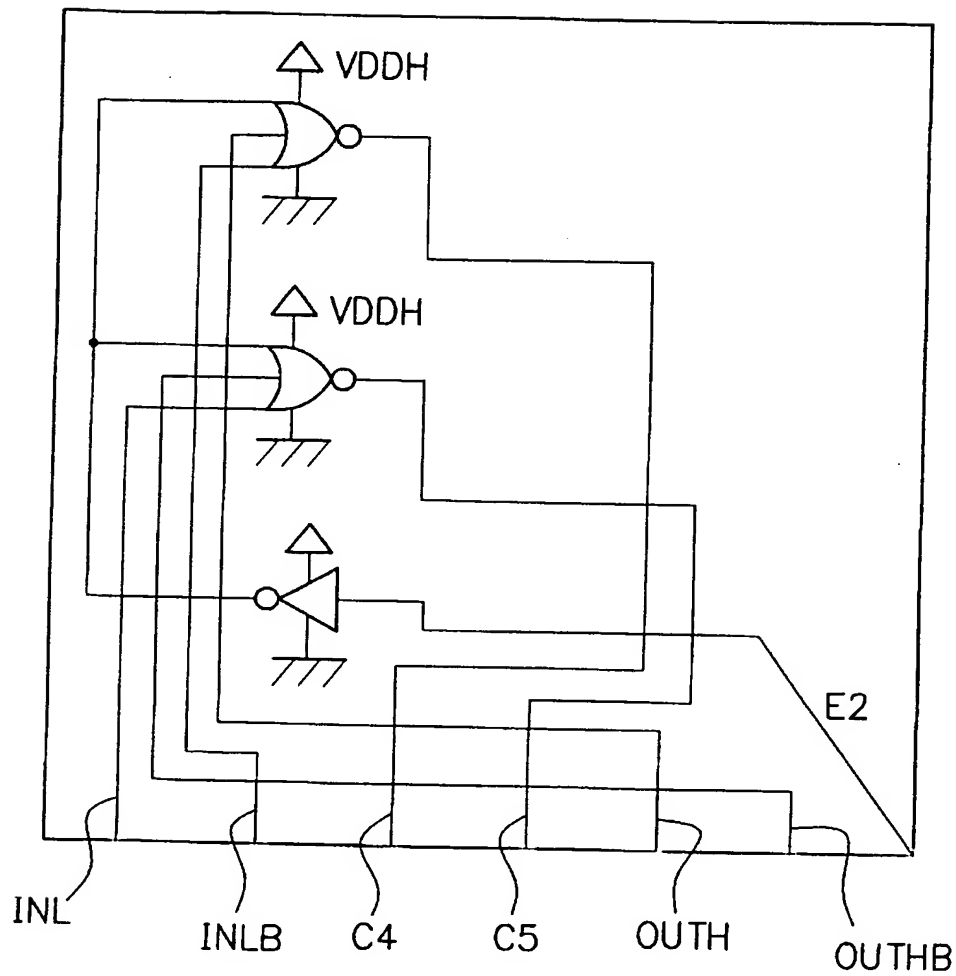




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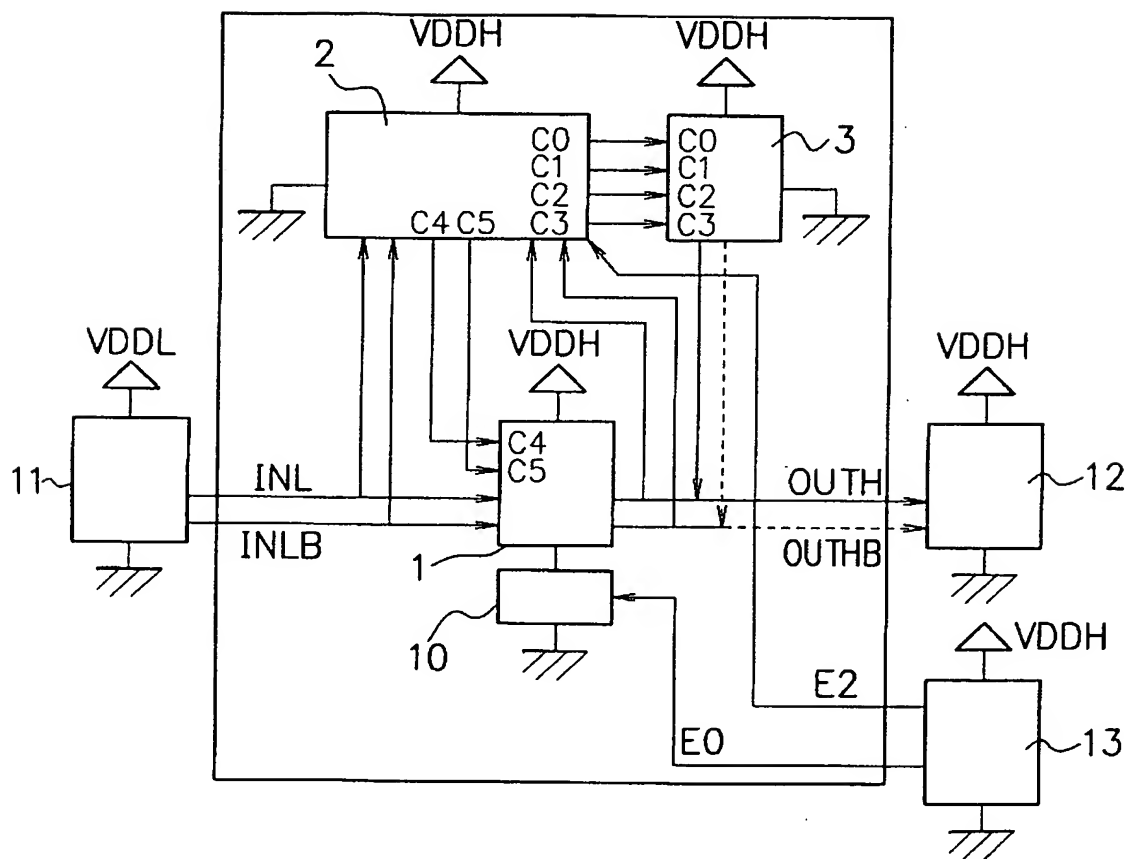
FIG.73



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FIG.74



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FIG. 75

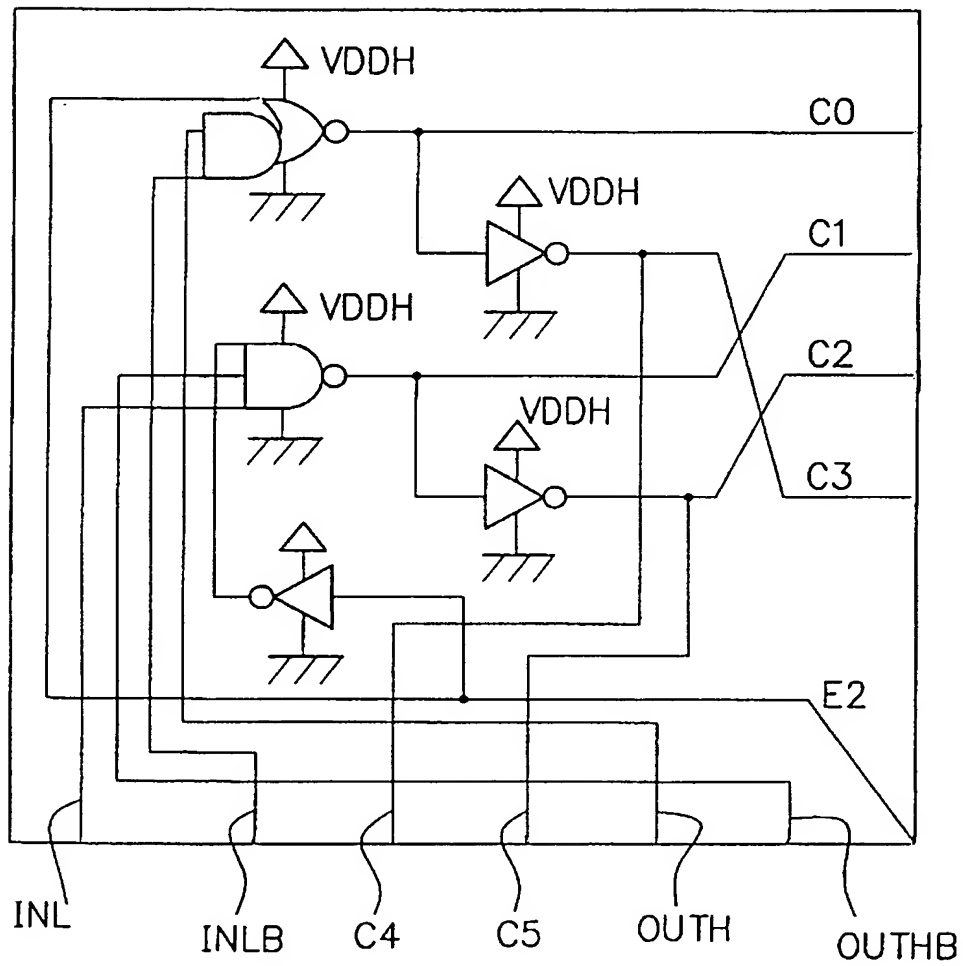
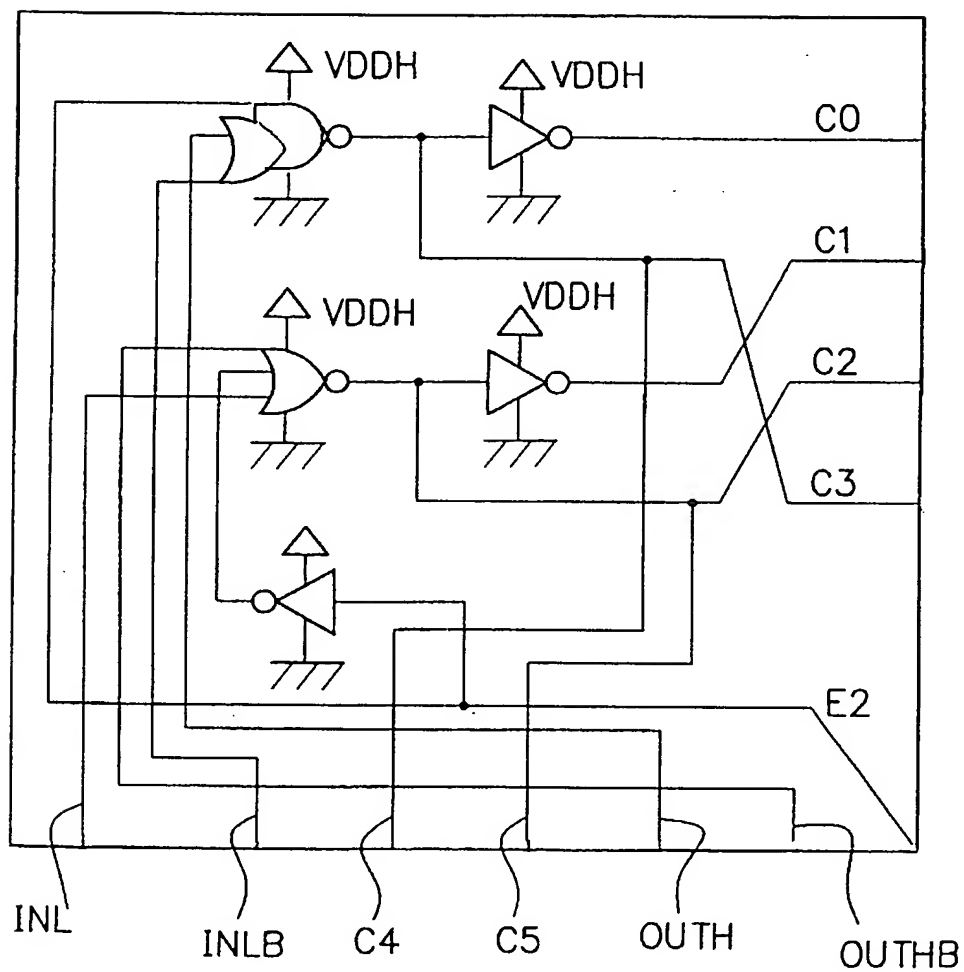


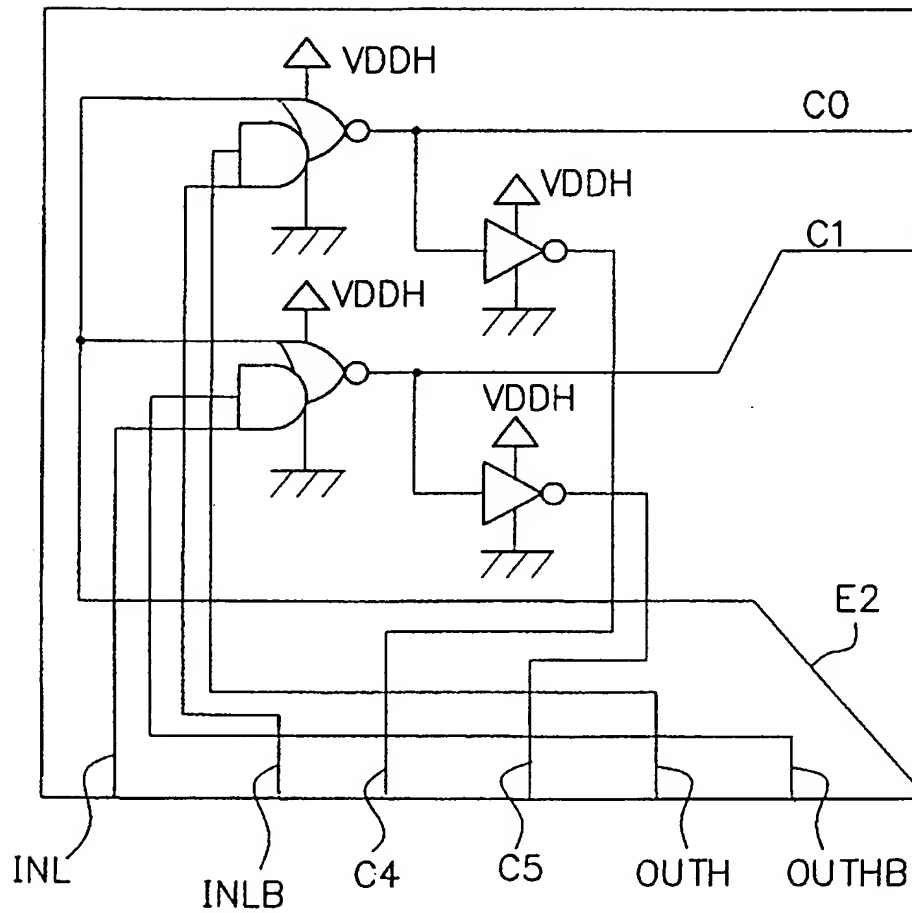
FIG.76



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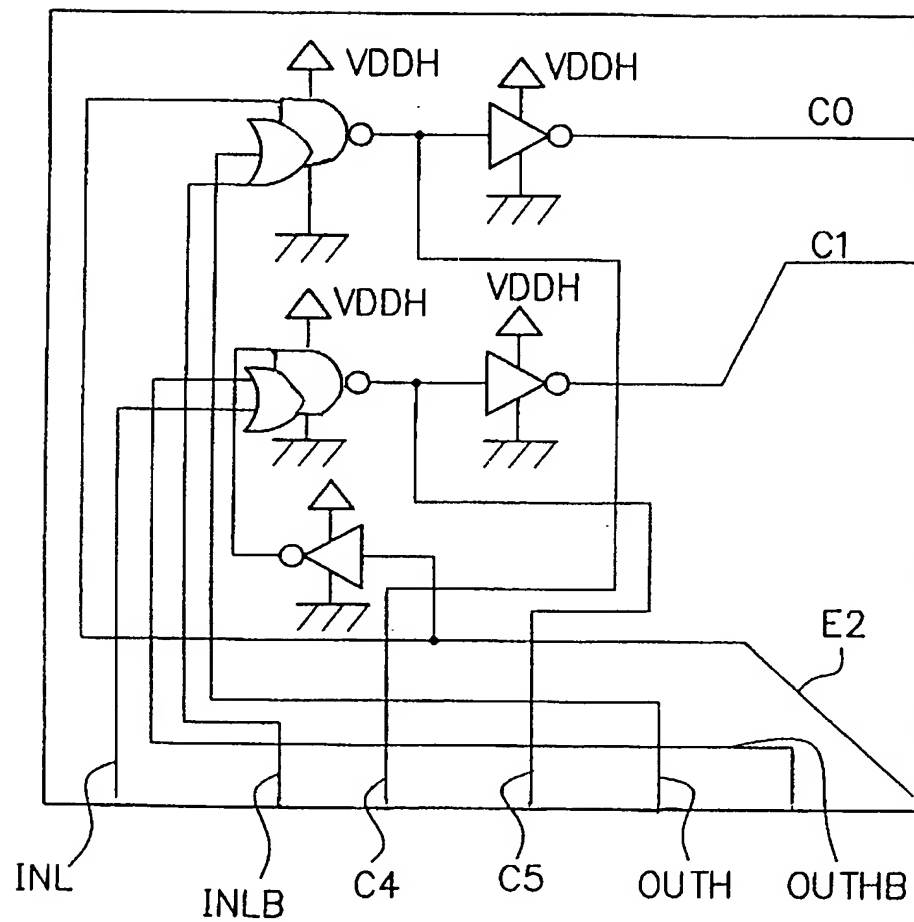
FIG. 77



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FIG. 78

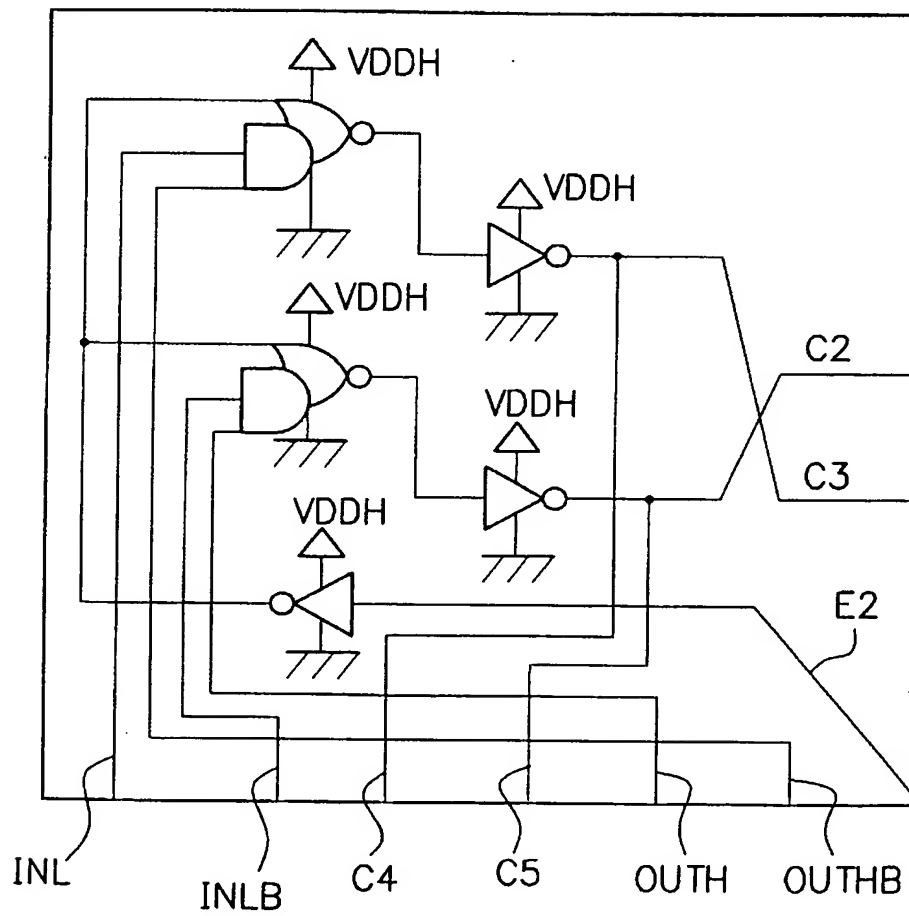


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National Stage Entry of PCT/JP2003/013931  
"A Level Shifter" - Filed on April 29, 2005  
Atty: Bernstein; Tel.: 202-293-7060  
Ref.: Q87822

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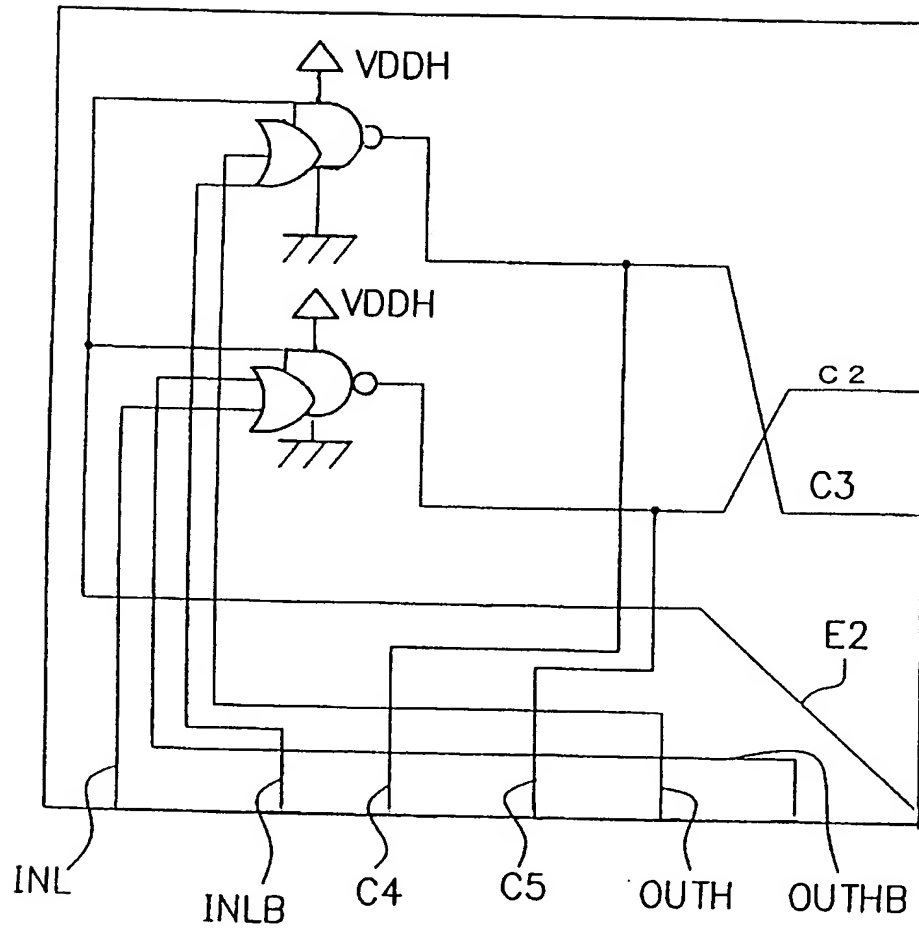
FIG.79



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FIG.80

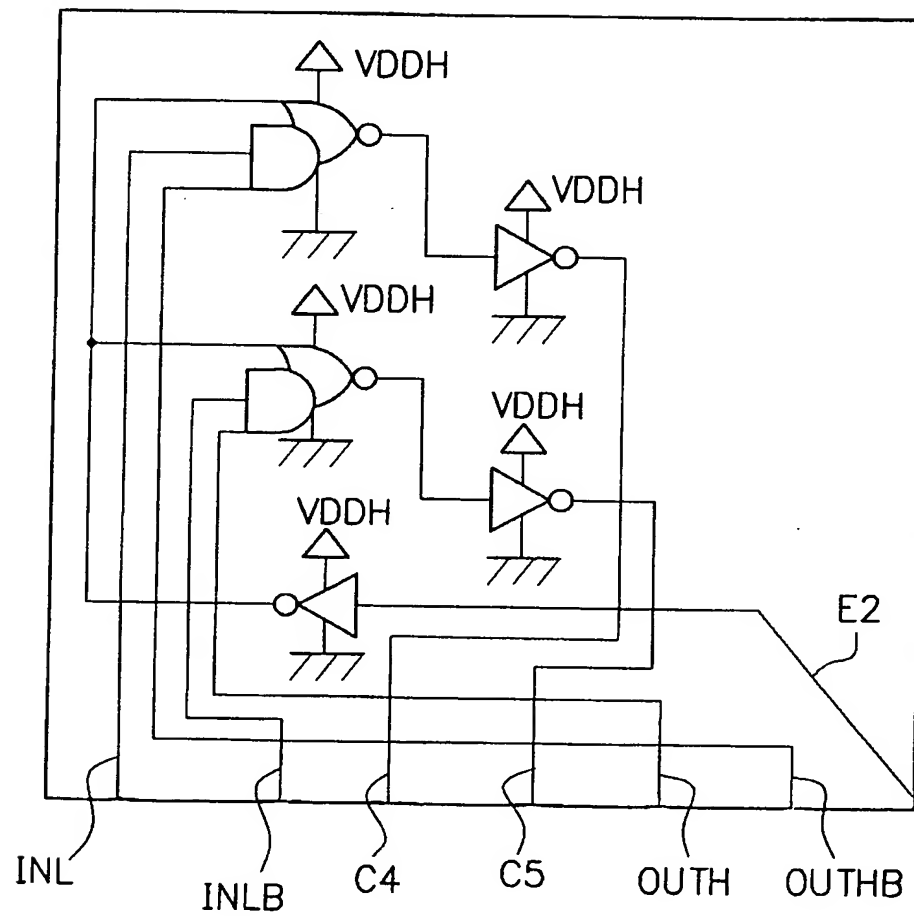




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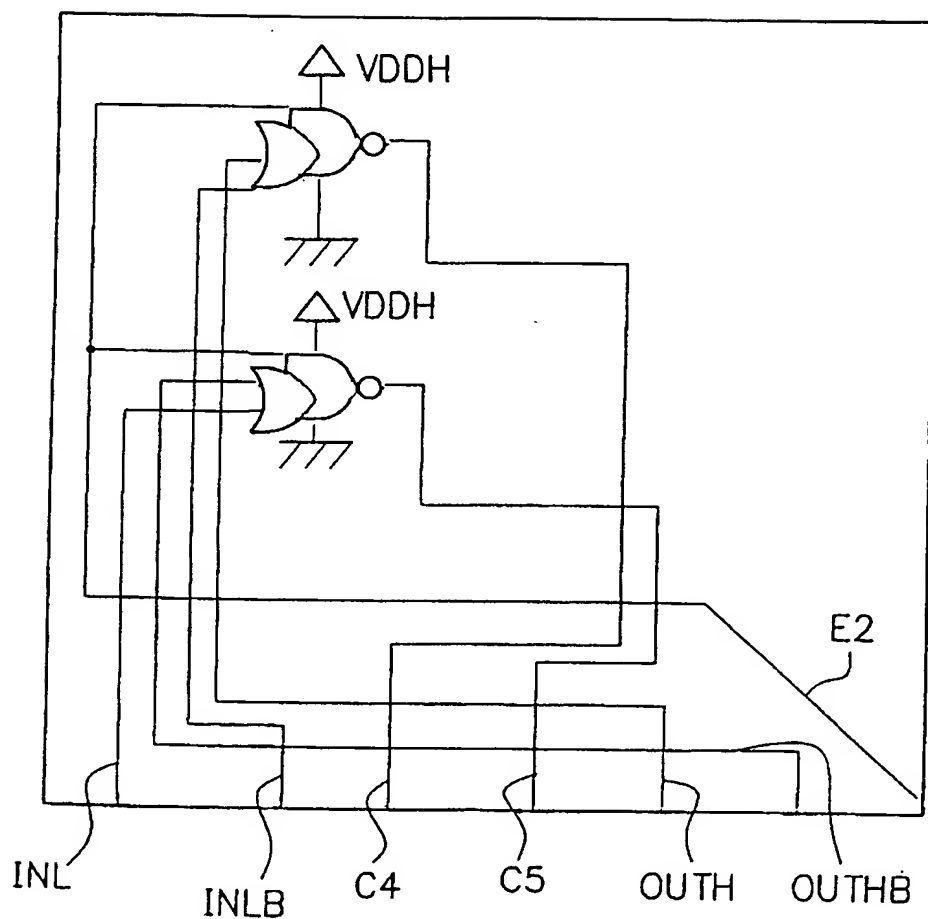
FIG.81



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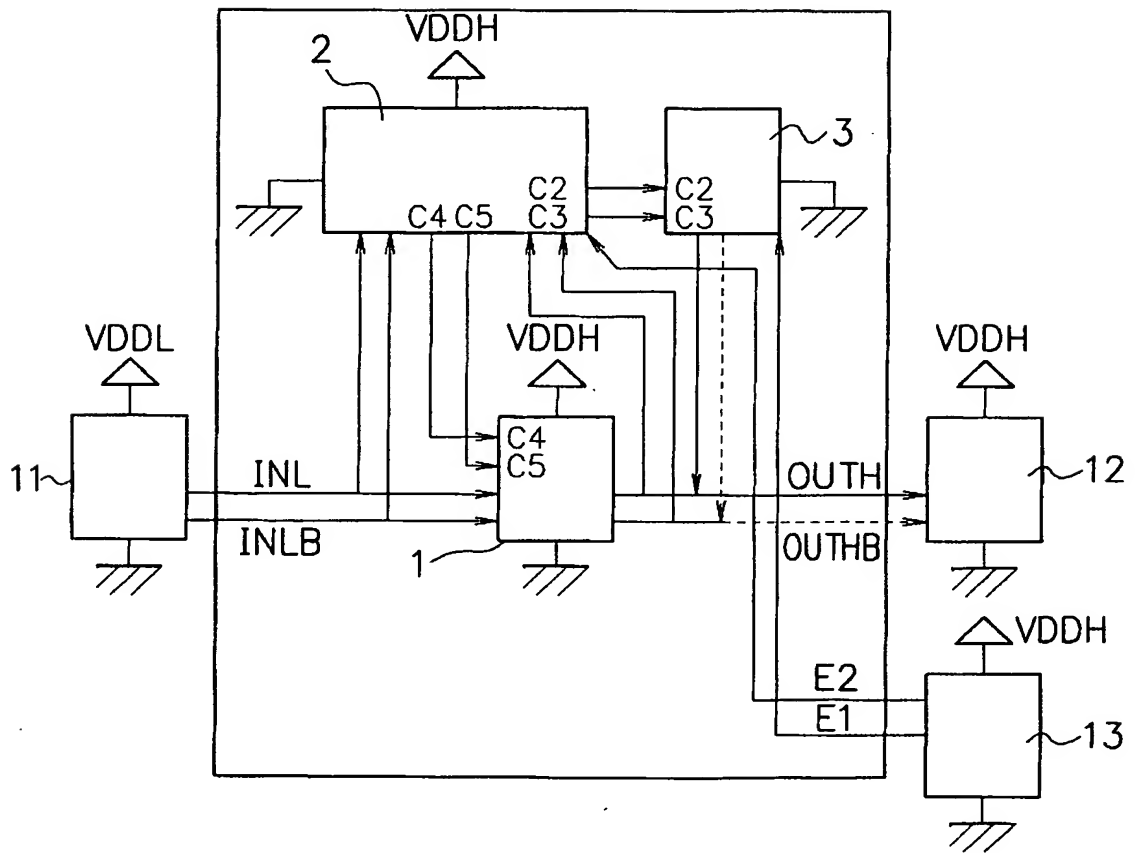
FIG.82



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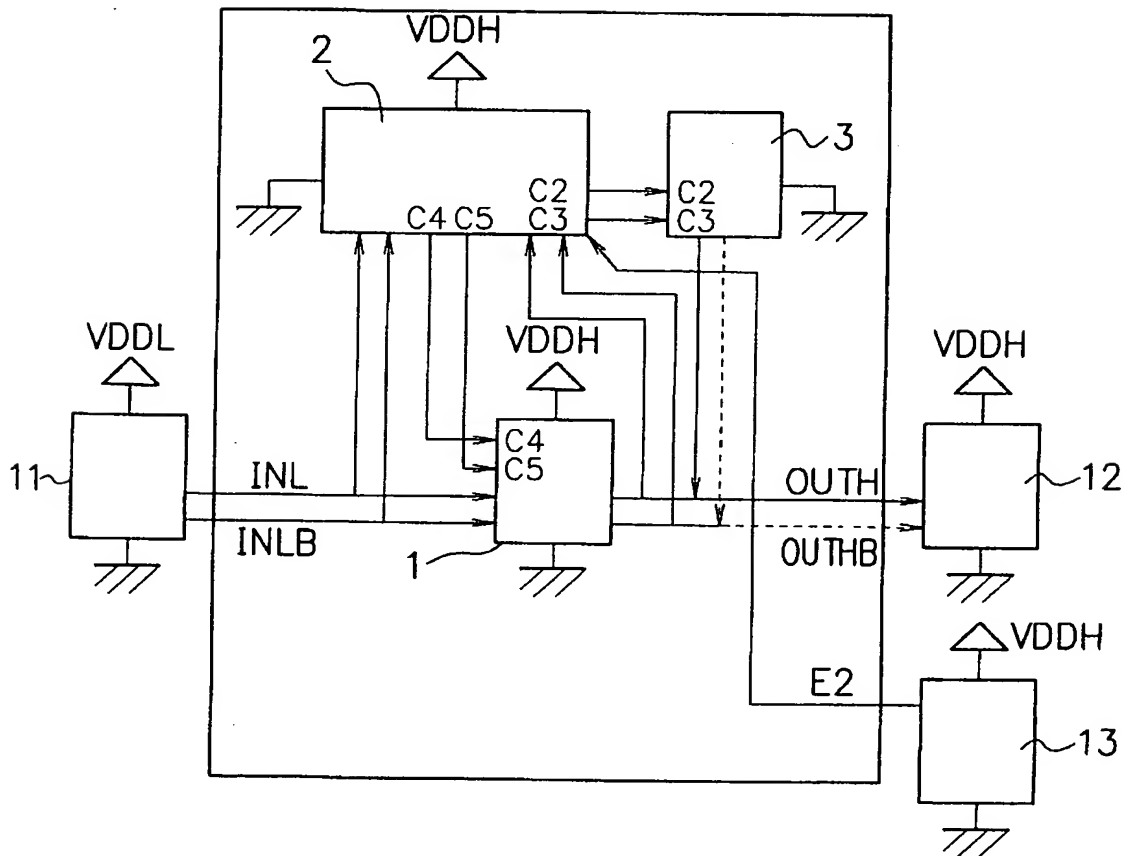
FIG.83



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FIG.84



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FIG.85

